A — 5 — 3 Formation of shallow P^+N junction by low temperature annealing

K. Yamada, M. Kashiwagi and K. Taniguchi

Toshiba Research and Development Center

Toshiba Corporation, Kawasaki, Japan

CMOS will be inherently well-suited for future VLSI devices because of its high switching speeds and large noise margins. At present, fabrication of high density CMOS devices requires a high conductivity P^+ region with very shallow junction depth.

This paper describes the lower limits of P^+N junction depth and activation temperature after B^+ implantation from a technological point of view. Two-stage model for the diffusion and activation of implanted boron atoms is also reported.

Under a wide range of experimental conditions (annealing temperature 600°C - 1000°C and time 5 sec - 180 min.), the diffusion of the implanted boron atoms during annealing can be classified into the following two stages. The first stage takes place within 10 sec and the second begins after the first finishes. The second stage diffusion is explained by a "four stream" model proposed by Chu(1). The first stage diffusion, in which the redistribution of boron during the annealing is very rapid and almost independent of annealing temperature from 600°C to 1000°C, cannot be described by the so-called "radiation enhanced" diffusion theory(2). An as-implanted boron profile for a dose of $5\times10^{15}cm^{-2}$ at 20 KeV is shown in Fig.1, along with 10 sec at 800°C annealed profile. Fig.2 shows P^+ junction depth as a function of annealing temperature and time. These results suggest that a low temperature process is effective for the formation of shallow junctions, but the junction depth is limited by the initial rapid redistribution of boron.

As shown in Fig.3, sheet resistivity after low temperature annealing of B^+ implanted layers is lowered by additional implantation of Si^+.

The rapid redistribution during the first stage of the anneal and the enhanced activation of B^+ implanted layers by additional implantation of Si^+ are explained as follows.

During annealing, solid phase epitaxial regrowth without an appreciable dopant redistribution starts from the interface between damaged zone and bulk toward the surface. As a result, within 10 msec, nearly 100% electrical activation of boron atoms are realized by high-dose B^++Si^+ implantation. Subsequent annealing makes the supersaturated boron concentration approach thermal equilibrium value by leaving lattice into substitutional sites. Therefore, in the first stage of annealing, the diffusion coefficient of boron are greatly enhanced via interstitial diffusion.

Two phenomena described above are less enhanced in the case of B^+ implantation because the damage from B^++Si^+ implantation causes a larger increase in configuration entropy compared with just B^+ implantation.

B^+ implantation allows the formation of high quality P^+N junctions with low leakage currents, even for low temperature annealing. Fig.4 shows the relationship between the leakage currents of P^+N junctions with B^+ and B^++Si^+ implantations for 60 min annealing. From this figure, we find that

the leakage currents for B^++Si^+ implantation are nearly equal to those for B^+ implantation. The leakage currents in the case of B^+(20 KeV) + Si^+(100 KeV) are, however, larger than those in B^+(20 KeV) + Si^+(40 KeV). These experimental results suggest that in order to obtain high quality PN junction with low leakage currents, the damaged layer produced by Si^+ implantation has to be within the junction depth.

In conclusion, the technique of B^++Si^+ implantation makes it possible to markedly reduce the annealing temperature of implanted layers. We have achieved a 59 ohm/□ diffused layer with a B^+(5×10^{15} cm^{-2} at 20 KeV) + Si^+(5×10^{15} cm^{-2} at 40 KeV) implantation and 60 min annealing at 600°C. The B^+ implantation has a limit of 0.25 μm for an acceleration energy of 10 KeV which is a lower limit of energy of commercially available implanter. This study suggests that B^++Si^+ implantation will be a necessary new technology for CMOS-VLSI.

References

(1) A.Chu, Stanford Electronics Laboratory Tech. Rep., No. 4969-2, 1977

(2) Y.Murikawa, H.Tsujii and K.Nagami, Inst. Phys. Conf., Ser. No.59, P.563, 1980

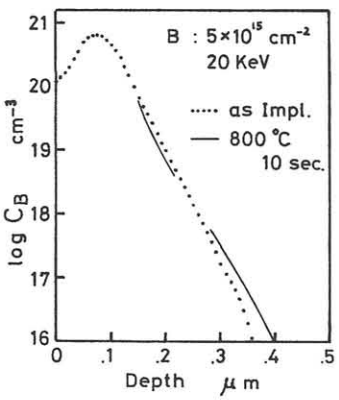


Fig.1 Boron profiles as measured with SIMS on samples without annealing and annealed for 10 sec.at 800 °C.

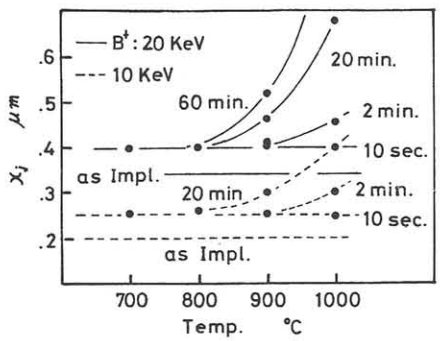


Fig.2 Relationship junction depth, annealing temprature and annealing time.

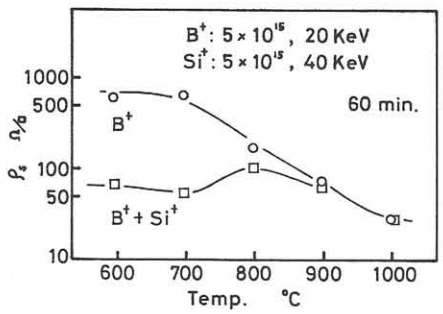
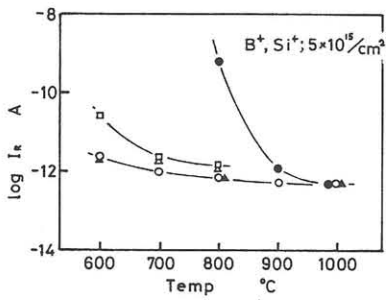


Fig.3 Enhanced annealing effects on B^+ implants following Si^+ implants.



Plots indicate ; (1) B^+ at 20 KeV, Si^+ at 100 KeV, ● . (2) B^+ 20 KeV, Si^+ 40 KeV, ▲ . (3) B^+ 20 KeV, ○ . (4) B^+ 10 KeV, Si^+ 25 KeV, □ . (5) B^+ 10 KeV, △ .

Fig.4 Reverse current of PN junction (200 × 480 μm) as a function of annealing temperature and time. For all curves, the reverse voltage is fixd at 5V.