A — 5 — 8 High Voltage Electron Beam Writing for Submicron Design Rule VLSI Fabrications

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Electron beam writing of VLSI devices with submicron design rules requires both the reduction of proximity effect and the improvement of the writing speed.

We demonstrate that high voltage electron beam writing virtually improves the writing speed in addition to the remarkable reduction of the proximity effect at a relatively low dose.

The formation of vertically walled resist patterns is known to be essential to the accurate patterning of submicron geometries. Figure 1 shows the dependence of a dose needed to develop a vertically walled submicron PMMA pattern upon electron beam accelerating voltage ranging from 20 kV to 50 kV. The dose needed at 50 kV is half the dose at 20 kV. On the other hand, the beam current increases in proportion to the accelerating voltage. As a result, the 50 kV acceleration yields 2.5 times the beam current at 20 kV. Thus, the high voltage electron beam writing at 50 kV ensures the improvement of the writing speed by a factor of 5, compared with conventional 20 kV writing.

Figure 2 shows that the proximity effect has been remarkably reduced by increasing the accelerating voltage up to 50 kV, as was reported previously[1]. It should be noted from a practical standpoint that the pattern size deviation from a designed value of 0.5 μm is within ± 0.05 μm irrespective of neighboring patterns, at a relatively low dose of 50 $\mu C/cm^2$ (50 kV) for 1 μm thick PMMA resist.

Figure 3 shows the formation of vertically walled PMMA patterns with an isolated 0.25 μm-space (top) and with arrayed 0.25 μm-spaces (bottom), written at 50 $\mu C/cm^2$ with a 0.25 μm diameter beam of 50 keV. The 50 kV writing realizes the simultaneous formation of the isolated and arrayed minimum spaces equal to the beam size.

MOSFET's with 40 nm thick gate oxide were irradiated by 50 keV electron beam with doses varying form 1 to 100 $\mu C/cm^2$. Figure 4 shows that the threshold voltage shifts due to the irradiation are reduced to small levels enough for MOS device application after 30 minutes annealing in forming gas at 450°C.

In conclusion, high voltage electron beam writing offers distinct advantage of higher speed writing of submicron design rule VLSI's in addition to the remarkable reduction of proximity effect without leaving significant amount of radiation damage to MOSFET's.

Reference:

1) T.R. Neill and C.J. Bull, Electronics Letters, vol. 16, No. 16, 621(1980).

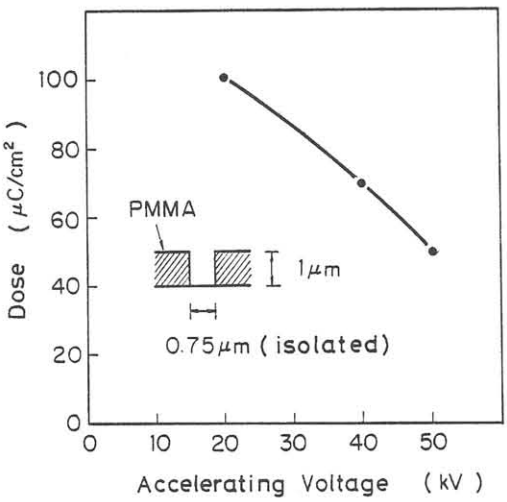

Fig.1 Doses needed to develop vertically walled resist patterns versus accelerating voltage.

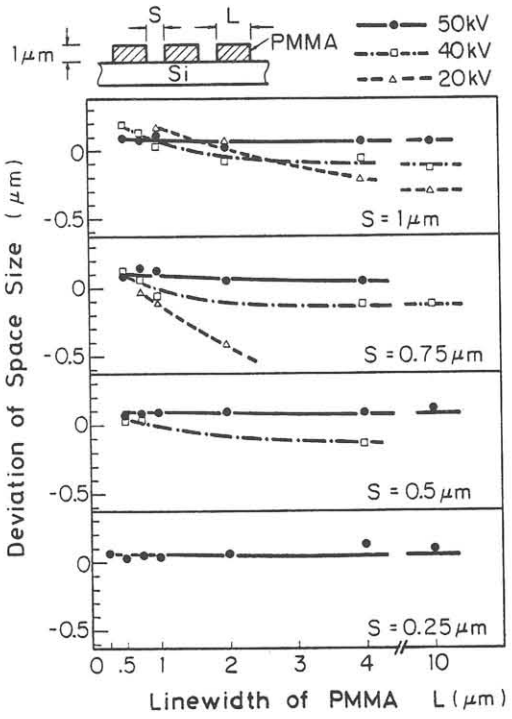

Fig.2 Reduction of proximity effect by high voltage acceleration.

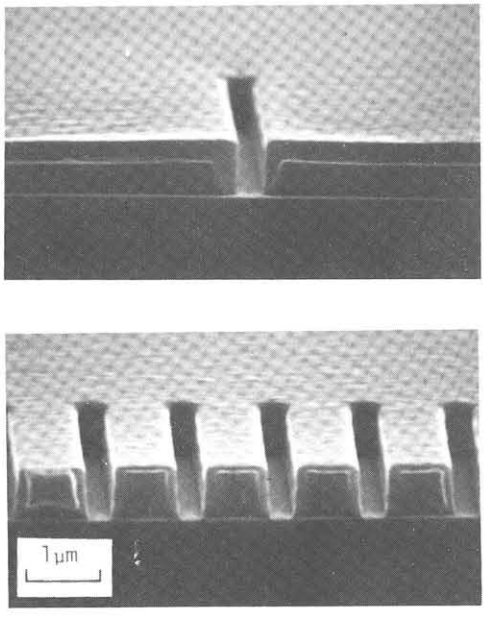

Fig.3 Vertically walled PMMA patterns: an isolated 0.25μm-space(top) and arrayed 0.25μm-spaces(bottom). 50kV-50μC/cm^2.

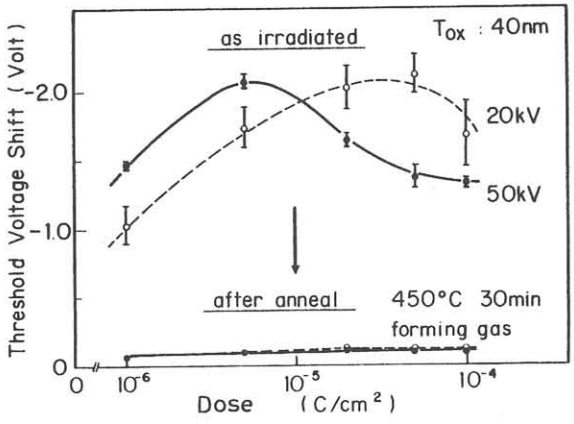

Fig.4 Threshold voltage shifts of MOSFET's due to 50kV electron beam exposure. The shifts are reduced to small levels after annealing.