A — 6 — 3

Radiation Damage in MOS Devices Underlying an Electron Beam-Annealed SOI Structure

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Beam annealing technology is attracting much attention for formation of Silicon-on-Insulator (SOI) structures[1], which have a potential application to three dimensional ICs. To realize large-area SOI, a shaped beam[2-3], especially, a line-shaped beam, is recommended, since a line-shaped beam could provide one directional heat flow and resultant one dimensional solidification of a molten silicon film. Use of electron beam (e-beam), compared with laser beam, is very attractive in this respect, since an e-beam can be easily formed into a desired shape, such as a line-shape and can provide higher output power to process a large area in one scan. One possible major disadvantage of e-beam annealing is damage creation. It is well known in e-beam lithography that e-beam irradiation with a charge density of $10^{-5} \sim 10^{-6}$ C/cm^2 introduces damage[4]. Since, in e-beam annealing, much higher charge density of $\sim 10^{-1}$ C/cm^2, 4 ~ 5 orders of magnitude higher than that in e-beam lithography, are used, damage of a very high degree could be created. On the other hand, by theoretical calculations, a high temperature rise, up to 1000°C or higher, is expected, for a certain period even after the e-beam is turned off. This e-beam induced heating (self-annealing) may eliminate the damage. At present, it is not well known which one of the processes, damage creation or self-annealing, predominates in e-beam annealing. Nor are the damage properties well known, provided that the damage creation process predominates.

This paper reports existance of a high degree of residual damage due to e-beam annealing in MOS devices underlying an e-beam annealed SOI structure, a quasi-three dimensional MOSIC structure. Use of a low energy e-beam is recommended based on results obtained for low temperature furnace annealing behaviors of device characteristics.

A cross section view of samples used in e-beam annealing is shown in Fig. 1. The MOS devices were fabricated by using the standard n-channel polysilicon gate process. Gate oxide films 40 nm thick, were grown in dry O_2 gas at 1000 °C. Thickness, t, from surface to gate oxide layer was changed from 0.9 to 3.9 μm. Electron beam annealing was accomplished at 20 keV (20 keV electron beam range R is 3.2 μm[5]) by scanning a cw-beam with a 80 μm diameter. Samples were fixed on a water-cooled Cu holder by using thermal compound. Scanning speed and overlapping ratio were 1.9 cm/sec and 80 %, respectively. After electron beam annealing, both SiO_2 cap and polysilicon film (SOI) on an isolation layer were etched off. Then, Al-Si electrodes were doposited by D.C. magnetron sputtering. Low temperature furnace annealing in H_2 gas was performed after Al-Si electrodes formation to study annealing behaviors of damage. The e-beam annealing influence was evaluated by MOS device characteristics measurement, using Qusai-static C-V method and I-V measurements.

Figure 2 shows the C-V curves for MOS capacitors in samples with t=3.9 μm (t_{si}=3 μm and t_{ox}=0 μm), therefore, for the t > R case. These measurements reveal the presence of a high degree of residual damage in MOS devices over the e-beam range, i.e., surface state creation and flatband voltage shift due to positive charge accumulation. Therefore, self-annealing in high power density e-beam irradiation is not sufficient to

anneal out damage created during e-beam irradiation, even though a temperature rise as high as 1000 °C or higher is expected from theoreical calculations. It is also noted that the shift in the C-V curve is smaller for the 76 kW/cm^2 case, where the SOI film is melted, than the 38 kW/cm^2 case, where the SOI film is not melted. Residual damage decreases with increasing furnace annealing temperature and is annealed out at 500 °C within the detection limit ($\sim 10^{10}$ 1/eV・cm^2 for the surface state density). In case of $t < R_p$, residual damage after furnace annealing changes with charge density penetrated through the gate oxides, as shown in Fig. 3. Low temperature furnace annealing (450～550 °C) is also effective, to some extent in this case, to reduce the damage. However, the annealing is not sufficient to completely eliminate the damage, if charge density which penetrated through the gate oxide layer is large. These results indicate that the properties of damage created by e-beam annealing are almost the same as in e-beam lithography.

In summary, the influence of radiation damage in MOS devices underlying an e-beam annealed SOI structure has been studied. A high degree of damage was observed to remain after e-beam annealing. However, the damage can be annealed out by low temperature furnace annealing in MOS devices over the e-beam range. Therefore, introduction of e-beam annealing technique in the MOS devices fabrication process does not bring about cruical problems, if low energy e-beam is chosen so that MOS devices exist outside the e-beam range.

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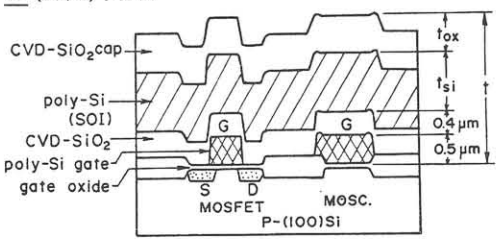

Fig.1:Cross sectional view of a sample used in e-beam annealing. tsi;poly-Si(SOI) thickness, tox;SiO_2 cap thickness, t;thickness from surface to gate oxide.

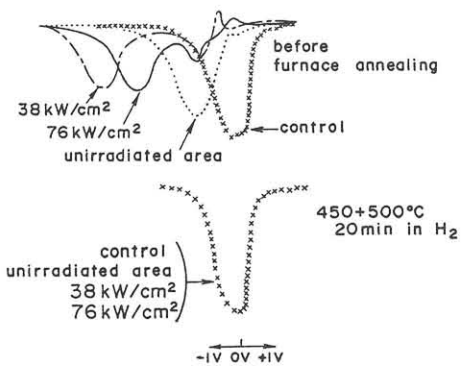

Fig.2:C-V curves for MOS capacitors in samples with t=3.9 μm (tsi=3 μm, tox=0 μm) before and after furnace annealing. Control;unirradiated sample, unirradiated area;unirradated area in an irradiated sample.

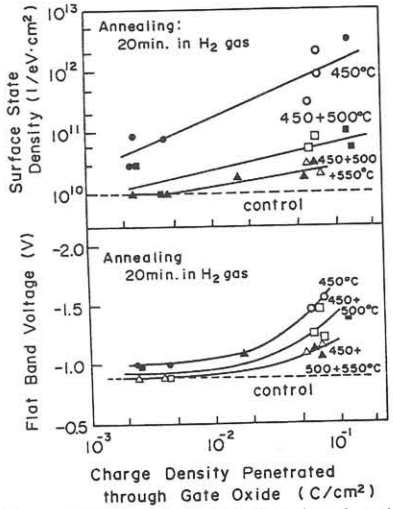

Fig.3:Surface sate density and flat band voltage vs. charge density penetrated through gate oxide. Open symbol;SOI was melted, closed symbol;SOI was not melted.