Characterization of laser-induced epitaxial Si crystals by evaluating MOS FETs fabricated in grown layers

M. Miyao, M. Ohkura, I. Takemoto, M. Ichikawa, M. Tamura and T. Tokuyama
Central Research Laboratory, Hitachi Ltd., Kokubunji, Tokyo 185, Japan

Recent work involving laser induced recrystallization of deposited poly-Si films on insulating layers is raising expectation of achieving new device structures using a Si-on-insulator (SOI) material system. The bridging epitaxy, i.e., seeded lateral epitaxy, proposed by the authors in 1980, is regarded as the most realistic approach when VLSI applications are considered. This is because precise control of the orientation of crystal layers grown over the insulator substrate is only possible through the seeding structure. However, detailed electronic properties of the grown layers have not yet been clarified, though preliminary evaluations of simple devices fabricated in the grown layers have been reported. This talk will describe the detailed characteristics of MOS FETs using them as device vehicles. Discussions will focus on the relation between structural and electronic properties of grown Si crystals.

In this work, a poly-Si layer was deposited on a Si substrate covered by SiO₂ stripes patterned 2 to 20 μm wide. Thickness of poly-Si and SiO₂ was set at 350 nm. A focused cw Ar scanning laser was used to melt the deposited poly-Si layer. Moving the laser spot caused the melted Si to first recrystallize epitaxially at the SiO₂ window area in contact with the Si single crystal substrate. This crystallization then propagated in lateral directions over the entire SiO₂ substrate.

Quality of grown layers was monitored by A-probe RHEED and TEM. Results are shown in Fig. 1 (a) and (b). Diffraction patterns in Fig. 1 (a) show that crystal orientation was identical to the various parts of grown layers. Thus, lateral epitaxial growth was confirmed. However, a TEM micrograph, Fig. 1 (b), indicated that dislocations were found in the layer near the SiO₂ edge. Etch pit observation showed that these dislocations extended to the surface region.

Diodes and MOS FETs were fabricated by a conventional process on the epitaxially grown layer. Forward diode characteristics were described by the formula; \( I = I_0 \exp(qV/kT) - 1 \) with \( n = 1.2 - 1.4 \). A \( 10^{-7} \) A/cm² reverse current level was obtained at 0.1 V. An example of the I-V characteristics of FETs is shown in Fig. 2, where a surface photograph and schematic cross-section are also shown. Gate oxide thickness, channel length and channel width were 53 nm, 8 μm and 15 μm, respectively. Channel mobility was 600 cm²/Vs. The inverse semi-logarithmic slope in the subthreshold region (tailing factor) was estimated at 90 mV/decade. These results were comparable to that of bulk Si and superior to the recently published data of a laser recrystallized poly-Si island surrounded by SiO₂.

This clearly indicated that the seeding process is essentially important in fabricating active device structures.

Channel mobility and threshold voltage \( (V_{TH}) \) of FETs were measured throughout the grown layers. They are summarized in Fig. 3 as a function of the distance of a gate region from the SiO₂ edge beneath the grown layer. Except for the region near the SiO₂ edge, channel mobility and \( V_{TH} \) values coincided with the expected values. The anomalous pit and peak at the SiO₂ edge are considered to be connected to the existence of the dislocations shown, and possible residual stress discontinuities near SiO₂ edge. Concentrations of 3 atoms implanted and annealed in the channel regions could be increased around such dislocations, causing the \( V_{TH} \) shift to a positive region.

In conclusion, single crystal Si layers grown laterally on SiO₂ substrate were shown to have sufficient electronic properties for VLSI fabrication. The importance of the seeding process is also indicated.
References

    and Appl. Phys. Lett. ( in press )
(5) H.W. Lam et al; IEEE (1980) EDL-1, 206

Fig.1 (a) Diffraction patterns of bridging epitaxial layer through μ-RHEED technique.
    (b) TEM observation near SiO₂ edge.

Fig.2 The I-V characteristics, photograph and schematic cross section of MOSFET fabricated on epitaxial layer on SiO₂.

Fig.3 Channel mobility and V_{TH} as a function of gate region position on bridging epitaxial layer.