A-6-8\* Evaluation and Control of Grain Boundaries in Laser-Recrystallized Polysilicon Island for Device Fabrication

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Silicon on insulator (SOI) structure consisting of Si films on an insulating layer is of interest as potential material for high speed CMOS-LSI and more complicated LSI applications<sup>1-3)</sup> as well as for a flat display panel application<sup>4)</sup>. Considerable effort has been done with the promising technique of c.w.-laser recrystallization of deposited polycrystalline silicon ( polysilicon).

This paper is concerned with the evaluation and the control of effects of grain boundaries on characteristics of MOSFETs fabricated on laser-recrystallized silicon films formed into device islands by using LOCOS technique before laser-irradiation. Also discussed is the result of fabrication of a nine stage ring oscillator with short channel MOSFETs.

The starting material was a 4 inch single crystalline silicon wafer with 1.1  $\mu$ m of steam oxide as an insulating layer. After deposition of 0.5  $\mu$ m thick polysilicon by LPCVD at 610 °C, boron ions were implanted with a dose of 1 x 10<sup>12</sup>/cm<sup>2</sup> at 50 keV in order to control the threshold voltage of MOSFETs. The polysilicon film in the field region was converted to thermally grown oxide using a LOCOS process. A device island was rectangular in shape, typically 75  $\mu$ m in length and 20  $\mu$ m in width. For a ring oscillator, the device island was 75  $\mu$ m in length and 6  $\mu$ m in width. After removing encapsulating layers on the polysilicon island, the laser-recrystallization process was performed by using a scanning c.w.-Ar laser with a spot size of about 50  $\mu$ m at the output power of 7.5 W. The scan speed was 12.5 cm/sec, the line to line stepping was 50  $\mu$ m and the substrate was held at a backside temperature of 450 °C. The gate oxidation cycle was timed to produce a 2000 Å thick layer of oxide on [100]-oriented silicon and resulted in a 3000 Å thick gate oxide on actual devices, which was measured by SEM observation. Successive fabrication steps were carried out by a standard N-channel MOSLSI technology.

Figure 1 shows the TEM micrograph of the laser-recrystallized device island. The recrystallized silicon was composed of long crystalline grains of about 5  $\mu$ m wide. Though some grains were originated from the edge nucleation, most of grain boundaries were elongated in almost parallel to the laser-scan direction. In the case of the laser scan along with a shorter side of the island, grain boundaries were also arranged parallel to the laser scan direction. The crystallgraphic orientations of grains were slightly different from each other, but they were found to be in rather near [111] than in [100] by TED observation. This result is consistent with the oxide growth rate on the laser-recrystallized polysilicon layer which was 1.5 times as high as that on [100] silicon, and with the interface charge state density of 4 x  $10^{11}/\text{cm}^2$  estimated from the electrical characteristics of MOSFETs stated below.

Figure 2 shows threshold voltages of MOSFETs as a function of nominal channel length, where the nominal channel width was 20  $\mu$ m. In the case of the laser scan direction parallel to the channel direction, the threshold voltage decreased remarkably for channel lengths below 5  $\mu$ m, and the number of devices with normal operation decreased due to excessive source-to-drain current. But in the case of the laser scan direction normal to the channel direction, short channel devices even at L=3  $\mu$ m exhibited the normal operation. These data well explains that the grain boundary diffusion of As from the source and drain regions into the channel during heat treatment caused the excessive leakage current and the decrease of an effective channel length<sup>5)</sup>. This also indicates that electrical characteristics affected by the grain boundary is controllable by the laser scan direction. Figure 3 shows the surface electron mobilities of devices as a function of nominal channel lengths in the case of laser scan normal to the channel direction. The effect of grain boundary on the mobility was clearly seen with the change of channel length. The maximum value of the mobility was calculated to be around 590  $\text{cm}^2/\text{V}$  sec by using the lateral diffusion length of As(0.15 µm) determined from devices on the single crystalline silicon. This value is very much close to that of devices in single crystalline silicon.

Taking into account of these results, a nine stage ring oscillator with an output buffer stage was fabricated. Each oscillator and a buffer stage consisted of an enhancement mode driver transistor with L=3  $\mu$ m and W=6  $\mu$ m, and an enhancement mode load transistor with L=15  $\mu$ m and W=6  $\mu$ m, whose gate was wired to its drain. Both transistors were fabricated in a same device island. Figure 4 shows the output waveform of the ring oscillator. Oscillations were consistently observed with a supply voltage of 17-20 V. This high operating voltage is due to high threshold voltages of both driver and load transistors. The minimum propagation delay was 38 nsec at Vdd=18 V, and the power-delay product was 82 pJ.

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Fig.1 TEM micrograph of the laser-recrystallized polysilicon island.



Fig.2 Threshold voltages of MOSFETs measured at 1  $\mu$ A of a source-to-drain current as a function of nominal channel length. The nominal channel width is 20  $\mu$ m.

(a) laser scan direction is parallel to the channel direction.

(b) laser scan direction is normal to the channel direction.

Fig.3 The surface electron mobilities calculated from nominal channel dimensions, observed gate oxide thickness and data of the transconductance curve with Vds=0.1 V. Laser scan direction is normal to the channel direction.



V<sub>DD</sub>=18 V

Fig.4 Output waveform of ring oscillator.