B—3—3 A New Short Channel MOSFET with an Atomic-Layer-Doped Impurity-Profile (ALD-MOSFET)

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It has been recognized that punch-through characteristics are the main problem in MOSFETs with gate lengths less than 1μm. Thus, there is a strong requirement for breakthroughs in both design theory and fabrication technology that will solve this problem.

Recently, a molecular beam epitaxy(MBE) technology was developed and has come into practical use. This paper proposes a new device structure featuring atomic layer-doped (ALD) impurity-profile fabricated by the MBE technique.

Application of the ALD structure to MOSFETs is schematically illustrated in Fig.1. The structure is shown to be favorable in developing very short channel devices with a submicron gate length.

Undesirable phenomena are known to exist in conventional MOSFETs with short channels, e.g., punch-through, threshold voltage shift, and soft breakdown. These phenomena are caused by (1) a two-dimensional current distribution, i.e., current flow dispersed into the depth direction near the drain (see Fig.2(a)), and (2) the saddle point in the electrostatic potential distribution approaches the source depletion region.

These two physical problems must be solved to suppress punch-through, threshold voltage shift, etc.

The new ALD-MOS structure, shown in Fig.1, is constructed with two heavily doped thin layers. One is situated close to the surface to suppress current flow penetration in the depth direction (see the current flow lines in Fig.2(b)). The other is situated deeper than the first layer to suppress expansion of the potential in the source direction. Potential contours near the drain expand to the source and the saddle point appears in conventional MOSFETs as shown in Fig.2(a). Thus, the second layer acts as a punch-through stopper, that is, potential contours are pinned near the drain. As a result, the two depletion layers caused by the source and drain p-n junctions are electrically separated as is shown in Fig.2(b).

Threshold voltage and tail constant in the subthreshold region are shown in Fig.3, as functions of effective channel length. It should be noted that the minimum channel length limited by the threshold voltage shift is in the submicron range. It is particularly significant that the tail constant remains almost constant even for 0.2μm. This shows that punch-through is completely suppressed

in the submicron range.

Drain breakdown characteristcs are shown in Fig. 4. Drain current in a conventional MOSFET increases sharply as a function of drain voltage, that is, a soft breakdown occurs due to punch-through. On the contrary, in the ALD-MOS, punch-through does not occur, and the breakdown voltage determined by avalanche multiplication is 14V.

Thus, ALD-MOSFET is a promising approach to realizing short channel devices in a submicron range. This paper provides guides for the device designs and fabrication technology.

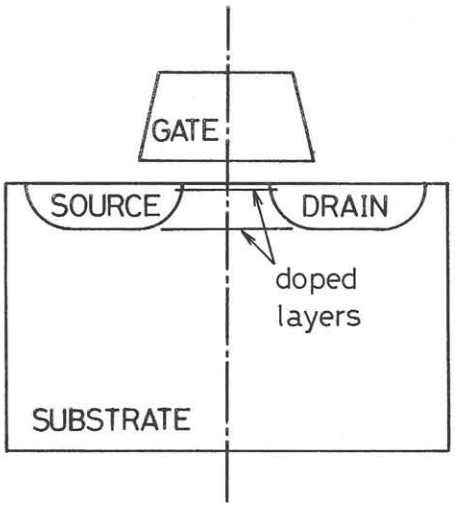

Fig.1 Crosssectional view of ALD-MOS.

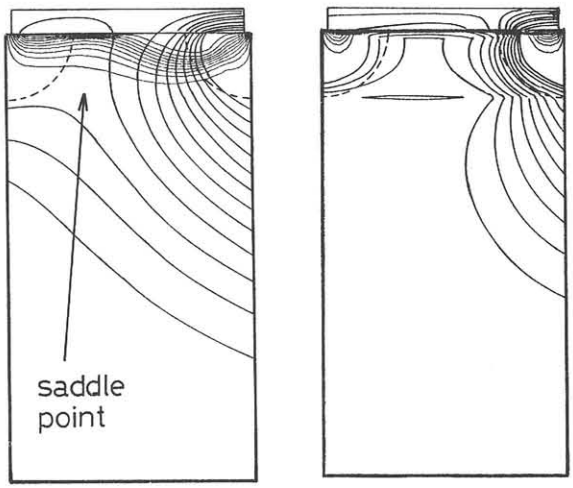

Fig.2 Potential and current flow distribution. (a) Conventioanl structure, and (b) ALD-MOS.

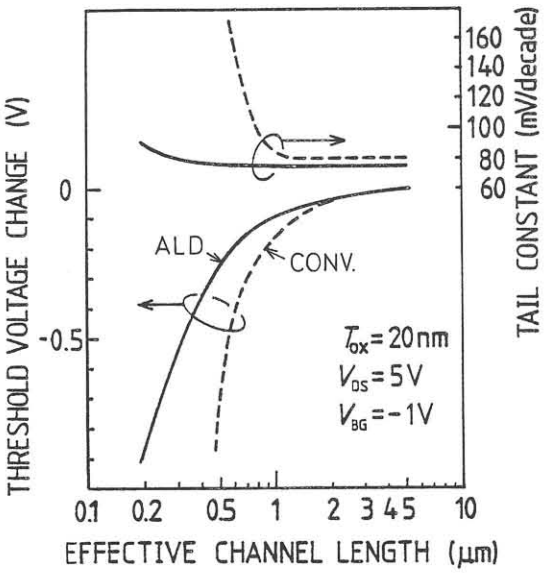

Fig.3 Threshold voltage and tail constant as a function of the channel length.

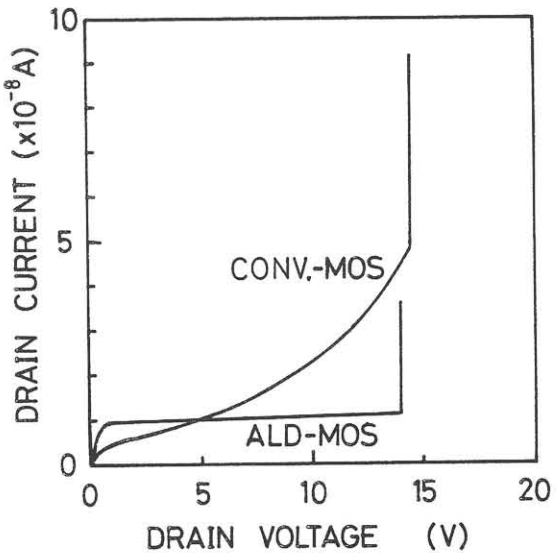

Fig.4 Drain breakdown characteristics of MOSFETs with L_{eff}=2μm and T_{ox}=20nm.