High-Speed E/D GaAs ICs with Closely-Spaced FET Electrodes

T. Furutsuka, T. Tsuji, F. Katano, M. Kanamori, A. Higashisaka and Y. Takayama
Basic Technology Research Laboratories, Nippon Electric Co., Ltd.
4-1-1 Miyazaki, Takatsu-ku, Kawasaki 213, Japan

Introduction

An enhancement/depletion mode (E/D) GaAs MESFET logic is being developed for achieving high-speed, low-power digital LSIs. In order to realize excellent performance on E/D GaAs ICs, the basic FET structure and the device pattern size have to be optimized. This paper includes the experimental results concerning FET structure and the performance dependence on device geometry. A 37.2 ps propagation delay ($t_{pd}$) was obtained with very low power dissipation ($P_d=261 \mu W$) from a 15-stage ring oscillator with submicron (0.4 $\mu m$) gate FETs.

FET Structure

A recessed gate FET structure has hitherto been widely adopted for reducing the unfavorable surface depletion effect1). However, such a structure may not be the best choice for large scale ICs. The closely-spaced electrode (CSE) FET structure (Fig.1), where the source-gate and the drain-gate spacings are shortened down to about 0.4 $\mu m^2$, has essentially no recess or steps on the GaAs surface. The CSE FETs exhibited 40-60% lower source and drain series resistances than the conventional recessed gate FETs1). This indicates that the unfavorable surface depletion effect can be effectively lowered by this structure. Gate breakdown voltage ($BV_{GS}$) and drain breakdown voltage ($BV_{DS}$) for the CSE FETs are: $BV_{GS}=-10 V$, $BV_{DS}>15 V$ for E-FETs and $BV_{GS}=-9 V$, $BV_{DS}>16 V$ for D-FETs, which are high enough for safe IC operation.

Device Geometry

Fifteen-stage ring oscillators (Fig.2) with different gate lengths ($L_G$) and gate widths ($W_G$) were fabricated on the same wafer. Lengths and widths of the interconnects were fixed for all oscillators. Active layers were formed by selective implantation of $^{30}Si^+$ into S.I. GaAs substrate2).

In Fig. 3, relationships between $t_{pd}$ and $L_G$ are shown, with $W_G$ as a parameter. In the case of relatively large size devices ($W_G=20 \mu m$), $t_{pd}$ was improved as $L_G$ became short, even in the submicron gate region. For small size devices, however, the reduction in $t_{pd}$ tends to saturate in the same region. This will be due to the
effect of stray capacitance. In wide $W_G$ or long $L_G$ case, the input capacitance for the next stage inverter becomes dominant. Propagation delay was found to follow the relation $t_{pd} \propto L_G^{1.5}$ in this case.

Dependences of $t_{pd}$ and $P_d$ on supply voltage ($V_{DD}$) for large size devices with different $L_G$ are compared in Fig. 4. It is seen that $t_{pd}$ can be effectively improved with small sacrifice of increase in $P_d$ by decreasing $L_G$. The minimum $t_{pd}$ of 34.1 ps was achieved at $V_{DD}=5.0$ V in $L_G=0.4$ $\mu$m/$W_G=20$ $\mu$m device. It is noted that this submicron gate device still operates at high speed ($t_{pd}=37.2$ ps) at $V_{DD}=1.0$ V with very low-power dissipation ($P_d=261$ $\mu$W).

Further experimental results concerning static and dynamic characteristics dependences on device parameters, and the performance of recently examined submicron gate E/D GaAs binary frequency dividers will also be presented.

Acknowledgment

The authors wish to thank Dr. H. Katoh for his support during this work and Mr. S. Asai for his useful advice regarding device fabrication.

References


Fig. 3 Propagation delay dependence on gate length.

Fig. 4 Speed-power characteristics comparison.