B — 5 — 2 An MSI GaAs Integrated Circuit using Ti/W Silicide Gate Technology

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Direct-coupled FET logic (DCFL) circuits with self-aligned enhancement/depletion GaAs MESFETs [1] are the most promising candidate for developing GaAs MSI/LSI circuits. A 4 x 4-bit parallel multiplier was fabricated as an example to demonstrate high-speed, low-power circuit performance.

A logic diagram of the 4 x 4-bit parallel multiplier consisting of 8 full adders, 4 half adders, 16 NOR gates and 16 input/output buffers, is given in Fig. 1. The IC was fabricated with a process that includes: (a) two selective implantation for FET channels, (b) sputtered Ti/W silicide gates, (c) high dosage implantation on both sides of the gates, (d) AuGe-Au ohmic contacts, (e) CVD SiO_2 between the first and second metal layers, and (f) Ti-Au interconnects. The circuit chip, shown in the microphotograph of Fig. 2, measures 1.5 mm x 1.3 mm in size including the contact pads, and contains 168 NOR gates with 2 μm gate length enhancement/depletion FETs. The mean values of the FET's threshold voltage were 0.17 V and -0.85 V, respectively.

The correct operation of the multiplier is demonstrated in Fig. 3, where S is a square wave pulse applied to the Y_1 input, and P's are the product outputs. To evaluate the operating speed, a full adder implemented ring oscillator was fabricated and tested. The propagation delay per gate (t_{pd}) which depended on the other input code (B, C) was in the range between 210 ps and 260 ps with the power dissipation of 0.36 mW/gate and the supply voltage of 1.5 V, as shown in Fig. 4. The maximum delay of 14 t_{pd} is expected for the Y_1 to P_8 data path, so that 4 x 4-bit multiplication will be performed in 3.6 ns, with the power dissipation of 54 mW at the supply voltage of 1.5 V.

In conclusion, the GaAs 4 x 4-bit parallel multiplier was fabricated using Ti/W silicide gate technology and was successfully tested. This indicates that more complex LSI circuits can be easily built by using the self-aligned FETs.

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[1] N. Yokoyama et al., "A Ti/W Silicide Gate Technology for Self-Aligned GaAs MESFET VLSIs", Tech. Digest Int. Electron Devices Meeting, Dec. 1981, pp. 80-83.

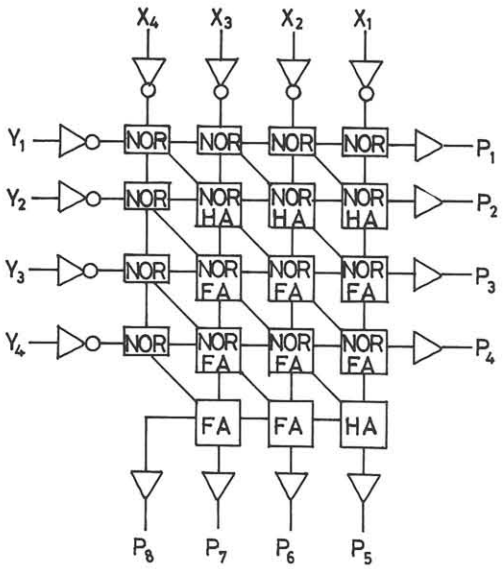

Fig. 1 Logic diagram of 4 x 4-bit parallel multiplier containing 168 NOR gates.

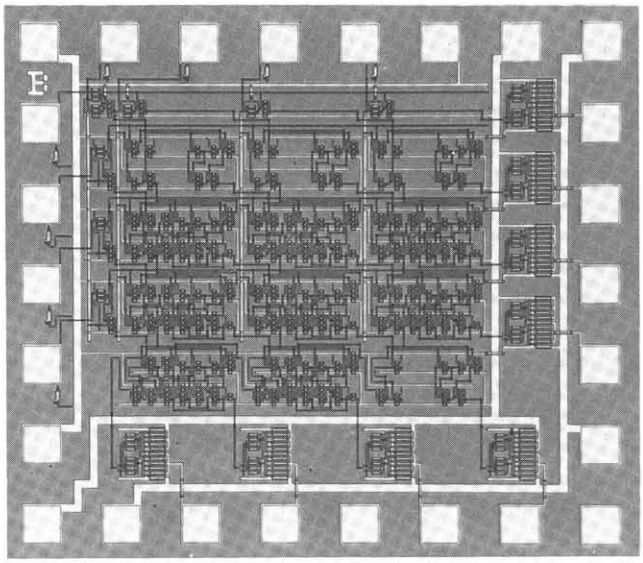

Fig. 2 Microphotograph of 4 x 4-bit multiplier. The chip size is 1.5 mm x 1.3 mm.

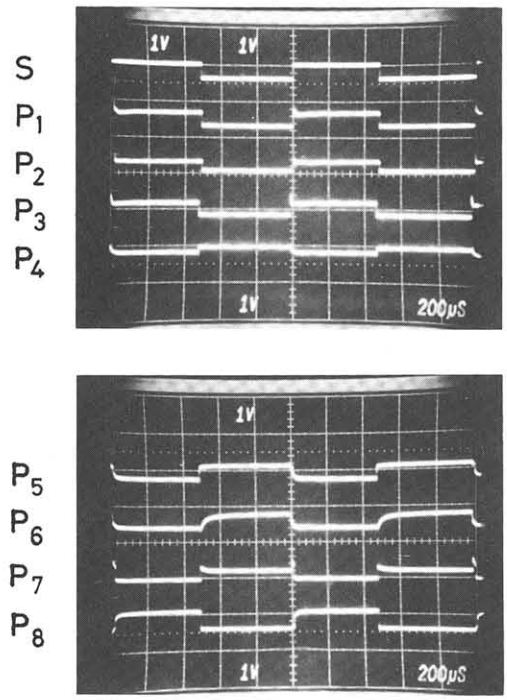

Fig. 3 Low-frequency operating waveform of the multiplier. The input code is 1111 x 100S = S$\bar{S}\bar{S}\bar{S}\bar{S}$SSS, where S is a square-wave input.

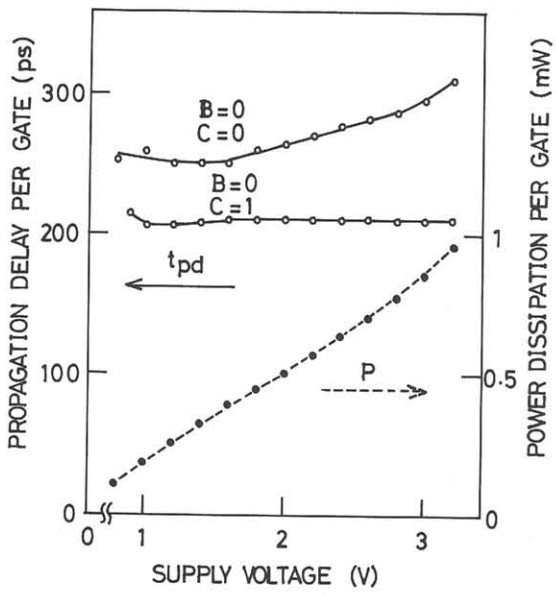

Fig. 4 Propagation delay time and power dissipation per gate as a function of the supply voltage.