B — 5 — 3 500 gates GaAs gate array

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As digital IC applications being more versatile, a great interest has been focused on semi-custom IC and LSIs. Among gate array families, ECL arrays enjoy the occupation of high speed devices. Typical propagation delay time and power dissipation are 0.5 - 1.3 ns and 1 - 5 mW per gate. GaAs logic is also one of the promising candidates for these high speed gate array families, smaller delay time and less power dissipation than ECL gates. However few studies have been reported except for BFL array.(1)

This paper first reports the intensive feasibility study for high speed GaAs DCFL gate arrays. Test device has 500 3-INPUT NOR gates, where 500 D-FETs and 1500 E-FETs are integrated, and realizes subnanosecond switching per gate.

Figure 1 shows a schematic drawing of basic cell. Table 1 is the typical device parameters and design rules. A unit gate is 3-INPUT NOR gate, consisting of 20 um wide driver E-FET and 10 μm wide active D-FET load. Gate length is 1 μm in mask pattern, and 1.4 - 1.6 μm in fabricated devices. Designed threshold voltages are 0.1 V for E-FET and -0.4 V for D-FET.

Generally gate arrays have periodic interconnection tracks even over the active device region, while tracks avoid the active transistor region in this GaAs gate array. A basic cell has 6 tracks perpendicular to and 4 tracks in parallel with transistor gate, power supply, and ground lines. Design rules are listed in Table.1. In addition to these tracks in a cell, 10 tracks are prepared among cell arrays. Total number of tracks will satisfy the requirements from ICs fabricated in this array. An example of test device is shown in Fig.2, which is the edge trigger T-FF.

I/O stages are indispensable in order that GaAs gate array is compatibly used with other logic gates. In this study the I/O circuit shown in Fig.3 is tentatively employed. Input buffer is DCFL inverters (W_g=40 μm, L_g=1 μm). Source follower D-FET and 3 level shifting diodes are prepared as output buffer, which are variously connected.

Gate arrays (chip size = 4.29 x 4.46 mm^2) were fabricated by Pt buried gate planar E/D process technology.(2)(3) Table 2 is the representative process parameters. Commercially avairable Cr doped 2" ϕ LEC wafer was used, from which about 100 chips are obtained. Active layers for E-FET and D-FET were formed by $^{28}Si^+$ selective ion implantation and successive capless annealing in AsH_3+Ar at 850^oC for 15 min. Threshold voltage was controlled by using Pt-GaAs solid phase reaction ever reported.(2) The standard deviation in one wafer was 56 mV. Interconnect metallizations were made by Ti/Pt/Au for 1st and 2 nd levels.

Typical performance ever obtained is summarized in Table 3. Propagation delay times for fan out = 1, 2, 3 gates were 0.22, 0.30, 0.39 ns for power dissipation of 0.1 - 0.3 mW per gate. Another

device performances (the dependence on the interconnection length, the number of crossover) will be presented in detail.

(Acknowledgment) The authors wish to thank Dr.R.NII for numerous suggestions. They are also grateful toMr.T. MIZOGUCHI, T. TERADA, M.HIGASHIURA, and S. SHIMIZU for helpful discussions.

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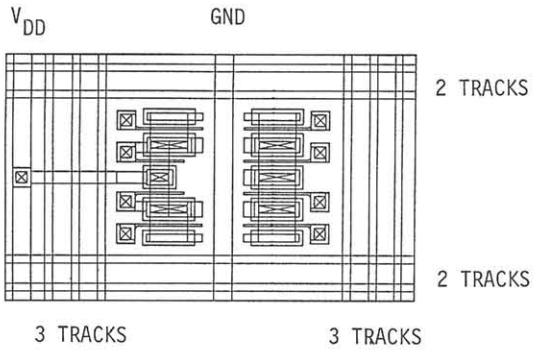

FIGURE.1 Basic cell pattern

TABLE.1 Device parameters and design rules

L_{geff}		1.4 - 1.6 um
W_g	(E-FET)	20 um
	(D-FET)	10 um
V_{th}	(E-FET)	0.1 V
	(D-FET)	- 0.4 V
$W_{1st,\ 2nd\ metal}$		4 um
$A_{contact\ hole}$		6x6 um^2

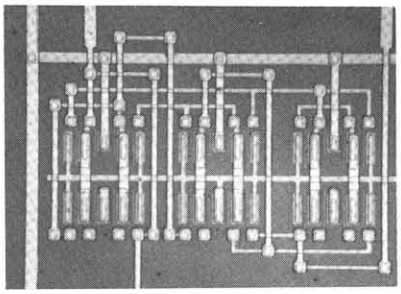

FIGURE.2 Edge trigger T-FF

TABLE.2 Process parameters

substrate		Cr doped 2"ø LEC wafer
active layer		$^{28}Si^{+}$ selective implantation
	E-FET	100 KeV 2.8 x 10^{12} cm^{-2}
	D-FET	150 KeV 1.8 x 10^{12} cm^{-2}
annealing		capless 850°C 15 min AsH_3-Ar
ohmic contact		AuGe/Ni 420°C 1 min alloy
gate metal		Pt(750 A) 400°C sintering
1st metal		Ti/Pt/Au
2nd metal		Ti/Pt/Au

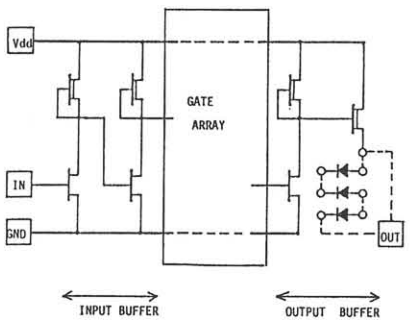

FIGURE.3 I/O buffer stages

TABLE.3 Typical performances per gate

Fan Out	1	:	0.20 - 0.23 ns	
	2	:	0.28 - 0.33 ns	0.15 - 0.25 mW
	3	:	0.36 - 0.42 ns	