B — 5 — 4 RECENT ADVANCES IN GaAs DIGITAL IC TECHNOLOGY*

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Interest in the GaAs digital integrated circuit (IC) technology is growing at a rapid pace. However, some controversy on the merits of a GaAs IC technology continues, particularly after recent high speed results obtained with submicron Si NMOS ICs. In this paper, a comparative analysis of the GaAs FET technology and Si technologies will be made. Material and processing advantages and limitations will be taken into account. The performances of the principal devices for different technologies (including the two-dimensional electron gas FET or HEMT) will be reviewed and compared. This discussion will be completed by comparing circuit performance data for several technologies.

Recent developments in GaAs IC technology at our laboratory will be discussed. This review will include MSI, LSI, and memory circuits. On MSI circuits, design criteria for frequency divider circuits aimed at obtaining high performance and high yield will be discussed. A Variable Modulus Divider having a simple D-flip-flop architecture and operating at a frequency as high as 1.84 GHz will be presented. This frequency of operation corresponds to an average propagation delay per gate of 109 ps which was obtained at a power dissipation rate of only 1.6 mW/gate. Yield as high as 65% was obtained for some wafers. The demonstration of the first GaAs digital LSI circuit, an 8 × 8 bit parallel multiplier composed of more than 1000 gates will be discussed. Based on the performance (5.25 ns multiply time), predictions on the performance of future GaAs LSI circuits will be made.

A new IC family would not be complete without memory circuits. New ideas for a very low power 4K GaAs static RAM will be presented. With a "power concentration" approach which saves power while the cells are not addressed, low static power dissipation is made compatible with high speed, for a low power, high speed radiation tolerant GaAs RAM. The design of the low power GaAs RAM cell which takes into account the low current regime of operation of FETs (subthreshold currents) and diodes, will be discussed. Experimental data demonstrating the operation of such a RAM cell at a static power dissipation rate lower than 1 μW/bit will be presented, along with preliminary results for 224 memory cell arrays.

Finally, an assessment of the prospects for the GaAs digital IC technology will be made.

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