B—6—2 N^+ Self-Aligned MESFET for GaAs LSIs

K. Yamasaki, K. Asai and K. Kurumada

Musashino Electrical Communication Laboratory, NTT.
Musashino-shi, Tokyo 180, Japan

Embedding n^+-layer at a controlled distance from gate contact has been realized in GaAs MESFET structure for the first time by developement of self-aligned implantation for n^+-layer technology (SAINT [1]). In the SAINT FET processing, n^+-layer is aligned to gate contact with a multilayer resist, which consists of bottom resist (FPM), sputtered-SiO_2 and top photoresist, as shown in Fig. 1. The sputtered-SiO_2 layer acts as an ion stopping mask for n^+-implantation (Si^+, 200 keV, $4x10^{13}$ cm^{-2}). The FPM pattern, which is made in an undercutting shape with respect to the upper SiO_2 layer by reactive ion etching, defines the gate contact region with the aid of lifted-off sputtered-SiO_2 pattern. The n^+-gate spacing can be arbitrarily controlled with the undercutting amount of the bottom FPM layer in the SAINT.

For n^+ embedded MESFETs, controllability and optimization of the n^+-gate spacing is of great importance. Because of lateral spreading of n^+-implants, too close n^+-layer to the gate contact results in gate capacitance increase and therefore in lowering of FET switching speed, which is proportional to product of gate capacitance and "on"-resistance. Contrarily, distance increase between the n^+-layer and gate causes "on"-resistance increase with switching speed down. In consequence, it is evident that an optimum distance might exist in the n^+-gate spacing from switching speed.

As the first step for n^+-gate spacing optimization, lateral spreading of the n^+-implants must be known experimentally to ensure that no anomalous phenomena occur. For this purpose, gate to source resistances were precisely measured with variation of the spacing from gate-side edge of n^+-implanted region to source-side gate edge. The spacing variation was made by use of shadow of the multilayer resist in connection with slight tilting of Si-ion beam scanning around 7° off-axis condition on (100) GaAs plane. The results shown in Fig. 2 verify that drastic improvement of series resistance outside the gate ceases at 0.28 μm of n^+-gate spacing, which is optimum in the light of device designability. Further shortening of the spacing causes the gate capacitance increase and unnecessary complexity of n-doping profile under the gate.

Threshold voltage controllability and in-wafer uniformity are required for MESFETs used in LSIs, especially for normally-off FETs in DCFLs (direct couple FET logics). Figure 3 and the Table show the gate length dependence of the mean

values and standard deviations of threshold voltages, which were obtained from 24 FETs for each gate length in a 6 mm x 9 mm area. When the gate length is shortened, slight threshold voltage shifts to negative direction were observed. The dependence might indicate the short channel effect necessarily associated with gradual increase of threshold scattering. However at leact down to 1 μm gate length, the threshold scattering of SAINT FETs is within margin of DCFL LSIs involving several thousand FETs [2]. It should be noted that the device characteristics are hardly altered by the first and second level metallizations as well as by the dielectric deposition. This electrical stability against the subsequent processing manifests the SAINT feasibility for LSI implementation.

SAINT fabricated FETs have remarkably large transconductance above 2 mS/10 μm gate width in the normally-off region. An E/D DCFL ring oscillator with 1 μm x 10 μm gate length x gate width shows a high switching speed of 45 ps/gate at a low supply voltage of 0.91 V.

In conclusion, flexibility to arbitrarily control the n^+-gate spacing has been realized with the proposed SAINT process, and the n^+-gate spacing has been optimized in terms of gate-source resistance.

References

[1] K.Yamasaki, K.Asai, T.Mizutani and K.Kurumada, Electron. Lett. 18 (1982) 119.

[2] M.Ino, K.Kurumada and M.Ohmori, IEEE Trans. Electron Device Lett. EDL-2 (1981) 144.

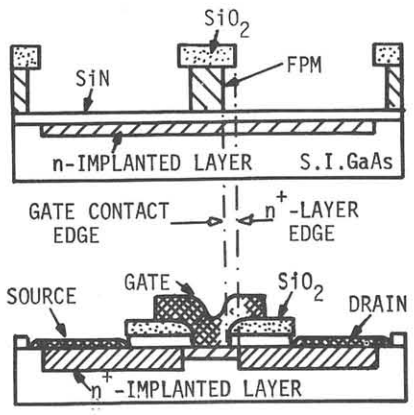

Fig.1. Cross-sectional views explainig relationship between multilayer resist shape and device structure (n^+-layers and gate contact).

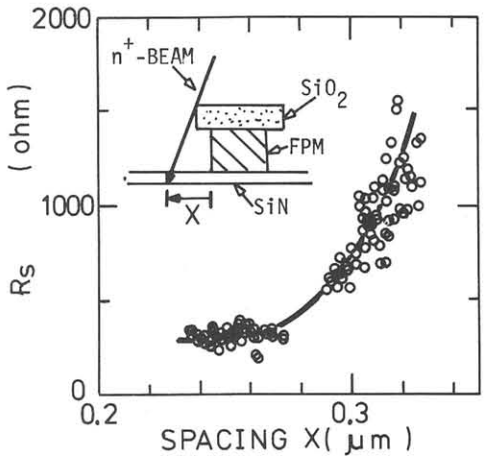

Fig.2. Gate-source resistance versus n^+-gate spacing. Gate width is 9 μm.

TABLE Mean values and standard deviations in threshold voltage for various gate lengths.

GATE LENGTH	THRESHOLD VOLTAGE MEAN	DEVIATION
1.0 μm	144 mV	34 mV
1.6 μm	194 mV	16 mV
2.0 μm	207 mV	9 mV

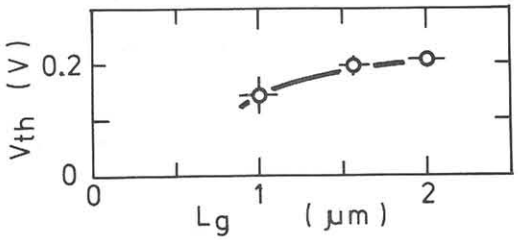

Fig.3. Gate length dependence of threshold voltage.