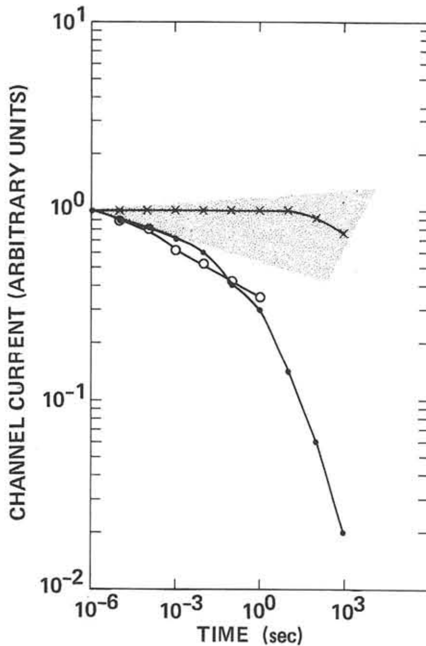
B — 6 — 4 The Effects of Interfacial Trapping on the Stability of MIS Devices on InP

D. L. Lile, M. J. Taylor and L. G. Meiners

Electronic Material Sciences Division, Naval Ocean Systems Center

San Diego, California 92152

Unstable device performance manifesting itself in hysteresis of C-V data and transistor output characteristics and in drift of threshold voltages and transistor channel currents with time is an ubiquitous problem which has historically confounded essentially all attempts to fabricate stable room-temperature operating MIS devices on compound semiconductors. Insulated gate devices have been reported recently on InP exhibiting promising characteristics for microwave applications with depletion- and enhancement-mode FETs,[1] surface channel CCDs,[2] and small-scale integrated circuits[3] having all been demonstrated with attractive high-speed characteristics. Despite these successes however, drift effects still exist for the InP/dielectric system which, it is generally believed, will severely hamper its implementation in any proposed system application.



Normalized plots of drain current vs. time following the application of an input voltage step to an InP MISFET. The shaded area encompasses the spread of data reported in Ref. 4 following severe surface etching with HCℓ. x - Present data; ● - Ref. 4, o - Ref. 5.

This paper will present results we have obtained on the time-dependent response of enhancement-mode MIS FETs on p-type and SI bulk single-crystal InP fabricated using a variety of surface preparation and dielectric growth processes. In particular, a cross-section of typically accepted methods of semiconductor surface preparation including the effects of pre-oxidation, of etching, of HCℓ reduction, of annealing, and of the use of SiO_2 versus $A\ell_2O_3$ for the deposited overlayer have all been addressed. The effects of the growth plasma and substrate temperature are also apparently of importance and their contribution to final device performance has been investigated.

It is evident that the data we have obtained does not support some of the models which have been previously proposed to account for drift in this system. The figure, for example, reproduces published results together with output current data representative of our best results obtained on an MIS FET mounted in a common drain configuration following application of a $0 \rightarrow +4$ v input step. It is clear that this device compares very favorably with the best performance previously reported and that its drift, although finite, is small. More significant however, is the fact that this particular transistor was prepared with no

surface pretreatment other than organic solvent washing and mild chemical etching prior to the deposition of the indirect PCVD SiO_2 dielectric.[6] In particular, no effort was made to eliminate or even reduce the surface native oxide.

These results, together with those on the effect of temperature, will be discussed in terms of a model in which drift in these structures results from injection of electrons into a disordered and probably inhomogeneous interface layer. This model predicts that the native oxide is not necessarily detrimental in the stability performance of these devices and that of more importance are such parameters as the cleaning procedure and the energetics of the dielectric deposition process employed.

Acknowledgment

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