B — 6 — 5 DESIGN CONSIDERATIONS OF COUPLING CAPACITORS IN GaAs INTEGRATED CIRCUITS

A.W.LIVINGSTONE and A.D.WELBOURN

British Telecommunications Research Laboratories

Martlesham Heath, Ipswich, Suffolk, England, IP5 7RE

Logic stages comprising GaAs depletion mode MESFETs are fast and simpler to fabricate than those using enhancement mode transistors. However, interconnection of depletion mode circuits requires level shifting circuitry which may be large, intolerant of process parameter variations and consume power. Passive interconnection of logic stages by capacitors has been proposed (1, 2) as a means of solving at least some of these problems.

The basis of capacitor coupling is shown in Figure 1 in which 2 inverters composed of depletion mode FETs are connected. When node A is high, node B is clamped by the forward bias gate current, and the capacitor is charged through Q2 to about 4.5V with a 5V supply. When node A moves to its low logic level a portion of the capacitor voltage is retained, taking the node B to a negative voltage, beyond pinch-off, turning off the second inverter. The voltage across the capacitor in this state is still greater than the magnitude of the FET pinch-off. While transferring from the high to the low condition the capacitor has to discharge the capacitance associated with the forward biassed gate of the second inverter. Thus the capacitor must be large, even at voltages beyond FET pinch-off.

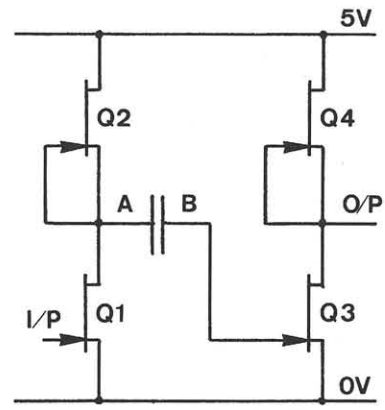

FIGURE 1

Of the techniques which could be used to fabricate the capacitors, we have chosen to use reverse biassed Schottky diodes which can be formed with the FET gates, thus simplifying manufacture. The capacitance of a simple, plane Schottky diode is shown as a function of bias in curve A of Figure 2. At the voltages of interest the diodes have very low capacitance, due entirely to the periphery of the diode. The reverse biassed capacitance can be maximised by making a high periphery diode as shown in curve B in Figure 2. Such diodes have been used and the photograph (Figure 3) shows a simple inverter with a high periphery diode to the left. The reverse biassed capacitance can be enhanced by making the capacitor pinch-off more negative than that of the FET. This can be achieved either by making the diode and transistor on different active layers, such as with dual implants, or by using a single active layer and recessing the transistor gates to reduce the total impurity concentration. Both of these structures involve a more

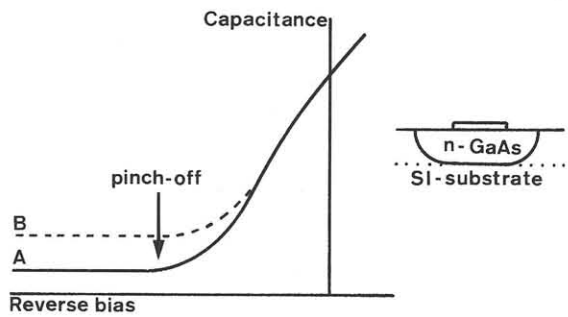

FIGURE 2

complicated fabrication process with consequent decrease in yield and process parameter control, and the exact form of the curves in Figure 2 has to be established before either can be used in a practial integrated circuit. In such a circuit the pinch-off voltages of both FET and capacitor can be modified by the back bias effect (3) from nearby electrodes. Although working circuits, including dividers operating above 1GHz, have been made using the structure shown in the photograph, more detailed design information was required. The 2 main concerns were: (a) the back bias effect which caused the capacitor pinch-off to move under the influence of adjacent circuit elements; (b) series resistance between the fingers of high periphery diodes. The effects were so important to capacitor-coupled logic that a test chip was prepared specifically for their evaluation. The chip had 36 different combinations of capacitor and adjacent back bias contact, the capacitors had varying sizes and finger aspect ratio and were made with various combinations of implant doses and energies. The back bias was provided by features on the wafer surface such as implanted areas, contacts and interconnection tracks corresponding to those which might be encountered within an integrated circuit of modest packing density. Test FETs were provided so that pinch-off voltage and saturation current effects could be quantified. Some inverters, with and without capacitor coupling, and with various back bias conditions, were measured to relate device performance to logic gate characteristics.

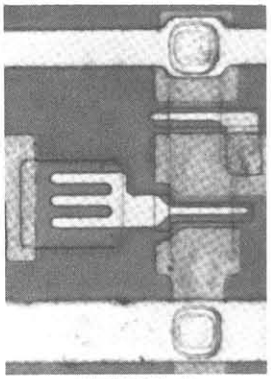

FIGURE 3

The purpose of the study was to identify the effect, on capacitors, of integration of reasonable packing density. The effect on the capacitor of other elements such as implanted areas, contacts and tracks has lead to design rules allowing full benefit to be obtained from the advantages offered by capacitor coupling on GaAs integrated circuits.

References:

1 Mellor,P.J.T., and Livingstone, A.W., "Capacitor-Coupled Logic Using GaAs Depletion-Mode FETs", Electronics Letters, 16, 19; 11 September 1980, pp 749-50.

2 Hashizume, N., et al., "Low-Power Gigabit Logic by GaAs SSFL", Electronics Letters, 17, 16; 6 August 1981, pp 553-554.

3 Rossel, P., et al., "Effects of the substrate bias on the Electrical Properties of GaAs FETs and Characterisation of the Interface between the Active Layer and the semi-insulating Substrate", Revue de Physique Appliquee, 13; October 1978, p 503.