C — 2 — 7 Josephson Full Adder Circuit Using Four-Junction Logic(4JL) Gate

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Josephson junction logic and memory circuits have been proposed and experimentally investigated as high performance computer elements. In various Josephson logic gates reported so far[1-5], direct-coupled logic gates are very attractive because of their small size and simple structure. We have proposed a new direct-coupled logic gate consisting of a closed loop of four Josephson junctions. The operating principles and the quasi-static operations of this gate have already been reported.[4] In this four-junction logic(4JL) gate, the switching characteristics are mainly determined by the phases of the four junctions, which allows us to eliminate inductances in the loop. The elimination of inductances in the loop makes it possible to reduce the gate size, resulting in small logic delay. In fact, a small logic delay of 20 ps/gate with an average power dissipation of 3.7 μW has been achieved in a 4JL gate chain.[6] In this paper, we report a Josephson full adder circuit consisting of the 4JL gates.

The full adder circuit design is based on two-input OR and two-input AND 4JL gates. Basic 4JL-OR and AND gates are shown with their symboles in Fig.1. An OR-gate is also used to provide current isolation between input and output for the AND gate. Exclusive-OR(XOR) gate consists of an AND and an OR gates controlled by a timing pulse. Input junctions(J_a, J_b) and resistors(R_a, R_b) in the AND gate are used for improvement of wider operating margin. Values of gate parameters are chosen to provide a wide operating margin of more than ±30% at gate-current levels in the circuit.

The full adder circuit diagram is shown in Fig.2. The circuit generates sum and carry outputs according to the logic function

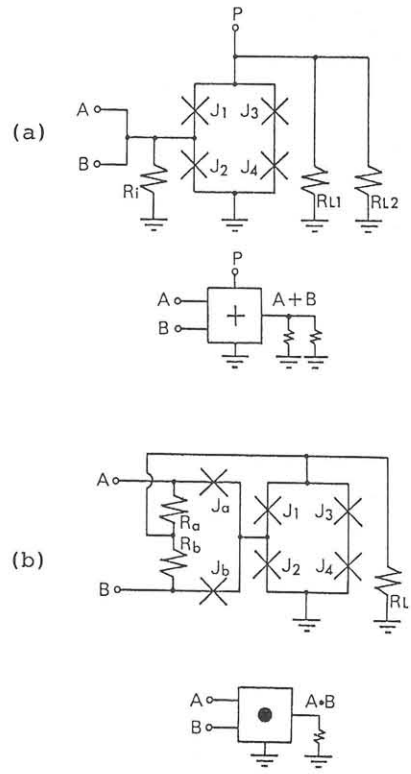

Fig.1. Basic 4JL circuits of (a)OR and (b)AND gates.

of Eq.(1). The sum output S_n is generated by a pair of XOR gates with the two timing pulses. The carry output C_n is generated by a combination logic circuit of the AND and OR gates. The full adder circuit requires bit signals(A_n, B_n) and carry(C_{n-1}), and two timing signals(T_1, T_2) from external circuits.

The circuit was integrated on a silicon wafer using a Pb-alloy junction technology with a 5 μm minimum feature size. Nb and Au-In films were used for the ground plane and resistors, respectively. Josephson current density was chosen to be 200 A/cm^2 to obtain a gate current level of 200 μA in the circuit.

Experiments were performed by applying power source(P), bit signals (A_n, B_n), carry(C_{n-1}) and timing signals(T_1, T_2) into the circuit. Figure 3 shows the input and output logic signal trains for the full adder circuit at a repetition rate of 2 KHz. As shown in Fig.3, a full adder function is consistently performed for the circuit as fabricated. The average gate current was 170 μA and total power dissipation was estimated to be 38 μW including current setting resistor power dissipations. A wide margin as predicted in the design could not be observed in the experiments. The reason is attributed to the variation of the junction critical currents.

We have demonstrated a full adder circuit using the 4JL gates as a new type of direct-coupled logic gate. The full adder circuit consisting of the basic 4JL-OR and AND gates was found to operate with low power dissipation of 38 μW.

$$C_n=(A_n+B_n)\cdot C_{n-1}+A_n\cdot B_n,$$
$$S_n=(A_n\oplus B_n)\oplus C_{n-1} \qquad (1)$$

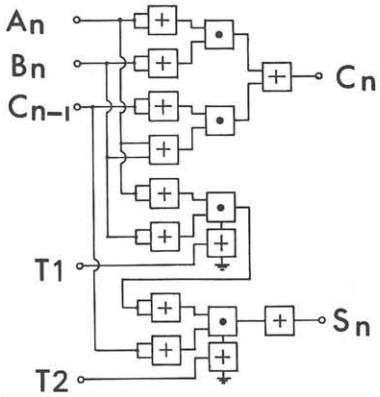

Fig.2. Full adder circuit diagram.

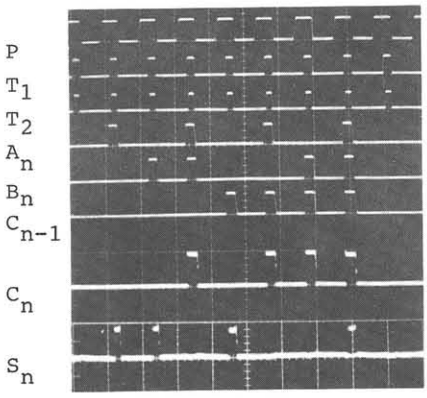

Fig.3. Input and output signal trains of the full adder circuit.

References

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