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Silicon TFT's for Flat Panel Displays

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Recent progress in amorphous silicon Thin Film Transistors (a-Si : H TFT) have stimulated considerable interest in active-matrix flat panel display devices. In these devices, the most attractive property is the dynamic memory distributed over the display area. The video voltage is now applied to the electrooptic transducer for a full frame period, instead of a line-time in a passive matrix system : an increased contrast is attempted. More generally, the final answer to the addressing problem, will be undoubtedly the complete integration of the peripheral driving circuits, improving compactness and reliability, and lowering the cost. Single crystal silicon I.C's have been successfully fabricated in this way. But for large-area, transparent and cheap devices, silicon TFT seems to be a more promising technology. Nevertheless, the a-Si : H TFT will be probably never used in a Video Phase Shift Register, because of its too low carrier mobility. Polycrystalline silicon TFT will be preferred in this case. This is the reason why we describe here a special TFT fabrication procedure, to get both amorphous - and poly - silicon TFT on a glass substrate. Static and transient response are then presented as well as a Liquid-Crystal Switching simulation. Finally, a 10^5 TFT matrix is shown and, therefore, the relevant technological problems are discussed.

Basic TFT Process

Two different TFT processes are described here, using either a low - or a high - temperature deposited amorphous silicon. Only the second process may include silicon recrystallization. Indeed, in the common a-Si : H ($T_s < 300^\circ\text{C}$), the hydrogen content amounts 10 to 15 at %, yielding cracks and bubbles after laser irradiation. Then, at low temperature deposition, only amorphous silicon TFT can be processed. In this case, silicon is deposited by a conventional plasma-enhanced C.V.D. technique on a common glass substrate, previously coated with metallic Source-Drain contacts. SiO_2 is deposited by the same way without vacuum breakdown. After Gate metal deposition, only one patterning operation is required to obtain the staggered TFT structure.

In the second process, amorphous silicon is deposited at a higher temperature ($T_s \sim 500^\circ\text{C}$) in order to minimize the hydrogen content (< 1 at. %). Then, silicon can be locally recrystallized by means of a CW or pulsed laser or a Flashlamp. A post-hydrogenation is performed to decrease the number of silicon dangling bonds. The final operations (SiO_2 , Gate deposition, patterning), are the same as above mentioned. By this way a-Si : post H and poly-Si : post H TFT's can be fabricated.

Static TFT characteristics

Polycrystalline TFT characteristics were previously reported. Field-effect mobility in the range of $15\text{--}20 \text{ cm}^2/\text{Vs}$ was obtained in a $0,1 \text{ }\mu\text{m}$ grain-sized polysilicon. In this paper, amorphous silicon TFT performances are extensively described. Source-Drain current-Vs-Voltage curves of both a-Si : H and a-Si : post H exhibit closely similar feature in the high-current region. Field-Effect mobility up to $0,2$ and $0,05 \text{ cm}^2/\text{Vs}$ respectively was routinely measured. The non-linear shape of the $I_{SD}(V_{GS})$ curve denotes a trap-controlled conductivity. The main difference between a-Si : H and a-Si : post H concerns the low-current region : at zero gate voltage the Source-Drain current is 10^{-13} and $5 \cdot 10^{-11} \text{ A}$ respectively. This could be explained by the fact that post-hydrogenation is governed by a diffusion law : the leakage current could take place at the less hydrogenated back-side interface (Silicon/Glass).

Transient response

In the active matrix, at TV rates, the TFT's should switch very quickly, and then, their transient response has been extensively investigated. Two main phenomena limit the switching speed.

First, a stray capacitance C_p (Gate/Source overlap) produces an extra current at every Gate signal front. In the L.C-TFT matrix display, the TFT's have been especially designed to minimize this effect ($C_p \ll C_{LC}$).

Secondly, the effect of traps was clearly emphasized in the transient response. When the gate is turned ON, a flux of electrons is emitted by the source electrode to fill the empty traps just passing through the Fermi-Level. The trap filling may spend up to 50 μs , depending on gate voltage and sample preparation. On the other hand, the turn-OFF time is always shorter ($\sim \mu s$). These specific times are shorter in a-Si : post H than in a-Si : H, suggesting a lower trap density in the first case. It must be pointed out that previous measurements of localized-states, led to a similar conclusion.

Liquid-Crystal simulation

These amorphous silicon TFT's were then studied as switching elements in an addressable L.C display. The liquid-crystal cell has been roughly simulated by an Op-Amp ($R_e > 10^{12} \Omega$, $C \approx 6$ pF). Assumption was made that no additional storage capacitance was needed. On the Video electrode (Column in the matrix) alternate frames were applied to suitable L.C operation. The gate voltage lied at - 5 V in the OFF state and + 15 to + 20 V in the ON state, and the pulswidth ranged 50 μs to 5 ms. This arrangement simulated operation of the device in a real multiplexed application.

It is worth noting that transistor operated either in the Source-follower or Drain-follower mode, depending on the frame polarity. The relevant TFT characteristic was then $I_{SD}(V_{DS})$ at $V_{GD} = \text{const.}$ or at $V_{GS} = \text{const.}$ The non-symmetrical shape of these curves yielded to an effective L.C voltage with a dC-component which would be balanced by a convenient back-electrode voltage.

Conclusion

Investigations of transient performances on amorphous silicon TFT's put forward the predominant role of localized states. The differences observed between two kind of amorphous silicon suggest that the defects would be mainly located into the semiconductor.

In addition to the physical study of elementary devices, construction of a large area circuit has been performed. This a-Si : H TFT matrix (320 x 320 pixels, 16 pixels/mm²), has been designed to address twisted Nematic Liquid Crystal. An excellent uniformity of film thickness has been reached (better than 5 % over the panel area). Yield evaluation is underway.

These results have been achieved by close collaboration with Michel Le Contellec, Joseph Richard, Madeleine Bonnel, Jean-Luc Favennec, Pierre Coissard, Michel Morel for the thin film physics and technology and with Bernard Grandjean and Philippe Weisse for the video application study.