C — 4 — 3 Electrical Properties of Polycrystalline Silicon MOSFETs on Glass

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Recently, polycrystalline silicon (Poly-silicon) thin-film transistors (TFTs) have been fabricated on glass substrates[1,2]. However, there are several disadvantages ; that is, poly-silicon deposition under ultra-high vacuum (1×10^{-10} Torr), difficulties in controlling the mode of TFTs and low field effect mobilities of TFTs. In this paper, we report the reduction of these problems and the improvement of electrical properties of poly-silicon MOSFETs.

The undoped poly-silicon films were e-gun evaporated onto the 0.8 mm thick and 50 mm square Corning 7059 glasses maintained at about 550 ^{o}C. The deposition rate was about 15 Å/sec and the pressure in evaporation was $1\text{-}5 \times 10^{-6}$ Torr. The poly-silicon films used in this experiment were about 0.4 μm thick and they had an <110> preferred orientation and a grain size of order of 0.15 μm. The sheet resistivity of undoped poly-silicon films was more than 10^{11} Ω/□.

Figure 1 shows the schematic structure of poly-silicon MOSFET, which is similar to the silicon on sapphire (SOS) device. After forming poly-silicon islands, the gate insulator of silicon dioxide (SiO_2) was deposited to a thickness of 1500 Å by chemical vapor deposition (CVD). The source and drain regions were formed by ion implantation and thermal annealing. For P-channel MOSFET (P-MOS), boron ions were implanted with 2×10^{15} /cm^2 at 60keV and the annealing was performed at 500 ^{o}C for 1 hour in dry nitrogen. For N-channel MOSFET (N-MOS), phosphorus ions were implanted with 2×10^{15} /cm^2 at 160 keV and the annealing was done at 500 ^{o}C for 20 hours. The sheet resistivities of these regions were less than 10^3 Ω/□. After forming aluminum electrodes to source, drain and gate area, MOSFETs were annealed at 380 ^{o}C for 30 min in nitrogen mixed with hydrogen

Figure 2 shows the drain current (I_D) vs voltage (V_D) characteristics of P-MOS and N-MOS. Both P-MOS and N-MOS are operating in enhancement mode. The threshold voltage (V_T) and the field effect mobility (μ_{eff}) of P-MOS in Fig.2 are -11 V and 8.4 cm^2/v.sec, respectively, and those of N-MOS are 8 V and 16.6 cm^2/v.sec. The field effect mobilities of MOSFETs having various channel lengths (L) and widths (W) are shown in Table 1. These values are calculated from I_D vs V_D characteristics in the saturation region. Size effects on the field effect mobility are observed for both channel length and width. The field effect mobility incerases with channel width and decreases with increasing channel length.

To evaluate the switching speed of poly-silicon MOSFETs, the propagation delay

(τ_{pd}) was measured from a ring oscillator. It consists of 21-stage inverters (β_R = 6) with fan-out of 3.5 and 3-stage output buffer inverters. Figure 3 shows the waveforms of the ring oscillator taken at the output node. The propagation delays vs supply voltage (V_{DD}) are shown in Fig.4 for P-MOS and N-MOS. The oscillation was observed at V_{DD} = -12 V for P-MOS and 9 V for N-MOS.

In summary, poly-silicon films which have the field effect mobility more than 10 $cm^2/v.sec$ can be formed on glass substrates by conventional e-gun deposition in high vacuum (1 x 10^{-6} Torr). MOSFETs fabricated on the poly-silicon films are operating in enhancement P-channel or N-channel mode. The propagation delay time per gate is less than 200 nsec.

References

1. M. Matsui et al, Appl. Phys. Lett., 37 936 (1980)
2. A. Misumi et al, IEEE IEDM Technical Digest 305 (1981)

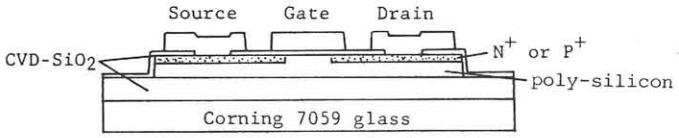
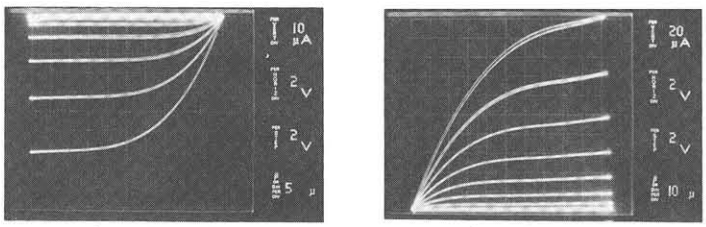


Figure 1 Schematic structure of poly-silicon MOSFET

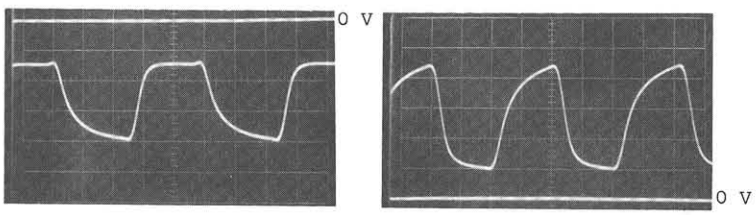
Table 1 Field effect mobilities of poly-silicon MOSFETs having various channel lengths and widths

Mode	V_T, V	μ_{eff}, $cm^2/v.sec$ ($\|V_D\|$ = 20 V)								
		W/L = 200/8	100/8	48/8	8/8	200/20	100/20	48/20	200/48	100/48
P-MOS	-11	11.4	12.0	11.1	10.6	8.4	8.1	7.7	7.7	
N-MOS	8	18.1	14.9	10.9	9.8	16.6	16.4		11.4	14.7



A) P-channel B) N-channel

Figure 2 Drain current and voltage characteristics of MOSFETs (W/L = 200μm/20μm)



A) P-channel
Vertical : 5 V/div
Horizontal : 5 μsec/div

B) N-channel
Vertical : 5 V/div
Horizontal : 2 μsec/div

Figure 3 Waveforms of 21-stage ring oscillator, $|V_{DD}|$ = 30 V (Inverter : $(W/L)_L/(W/L)_D$ = (8μm/8μm)/(48μm/8μm))

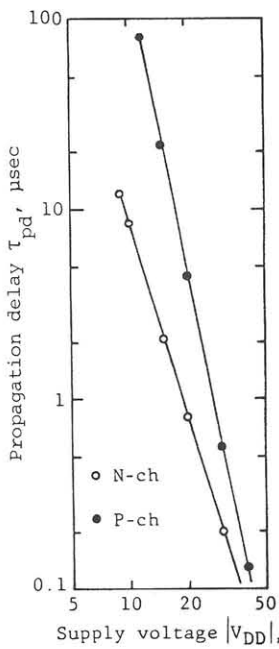


Figure 4 Porpagation delays vs supply voltage