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(Invited)

FUNCTION-TESTING OF PASSIVATED LSI'S WITH STROBOSCOPIC SCANNING ELECTRON MICROSCOPE

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The stroboscopic scanning electron microscope becomes a powerful tool to function-testing of semiconductor devices. It has ~~the~~ higher spatial and temporal resolutions than a mechanical probe. The time resolutions of short picoseconds have been already reported. The various devices, Gunn devices, microwave ICs, LSIs, surface acoustic wave devices, have been tested by several groups.

We shall review the principle of a stroboscopic SEM and its applications to semiconductor devices. Then we shall report the method and result on function-testing of the microprocessor 8085A with passivation (case A) and without it (case B) by using the phase-stepping image mode. Function-testings by using the waveform mode for the other LSIs with passivation has been already reported elsewhere.[1,2]

When an insulator is observed with a SEM, the contrast disappears from the screen of a CRT due to the surface charge-up. The SEM micrographs can be taken, however, if the accelerating voltage of electrons is low and if the measurement is done within τ. τ depends on many factors: the electron beam current density, the secondary-electron emission yield, the capacitance and EBIC between the surface and the inner electrode, the surface leakage and so on. In our case, τ (sec) $\sim 2*10^{-3}/$(electron current density (A/m^2)).

The logic-mapping mode has been used to display the logic state at a certain fixed scanning line (Fig.1(a)).[3] Here the phase-stepping image mode is proposed. The scanning line moves vertically as shown in Fig.1(b). The image contains the two-dimensional information as well as the phase and the charge density deposited on the surface is much less than the former.

Figs.2 and 3 show the stroboscopic micrographs of some parts of a uP 8085A. Fig.2 is for case A and Fig.3 for case B. Experimental conditions are shown in Tables I and II. Fig.3 shows a usual voltage contrast; the brighter part corresponds to the lower voltage and vice versa. On the other hand, in Fig.2, variations of voltage are displayed; the brighter or darker part corresponds to the raising or dropping voltage respectively and the gray part means no variation of voltage. (See the encircled region of Figs.2(d) and 3(d).) The measured time properties for case A agree well with the ones for case B within the experimental error of $\pm$ 5 ns as shown in Table III.

References (Full ones will appear in the Proceedings.)
1. H.Fujioka,K.Nakamae and K.Ura, IEEE J.Solid-State Circuits,SC-15,177(1980)
2. K.Nakamae,H.Fujioka and K.Ura, Trans.IECE Japan,64C,893(1981)
3. P.Fazekas,H.P.Feuerbaum and E.Wolfgang, Electronics,105(July 14 1981)

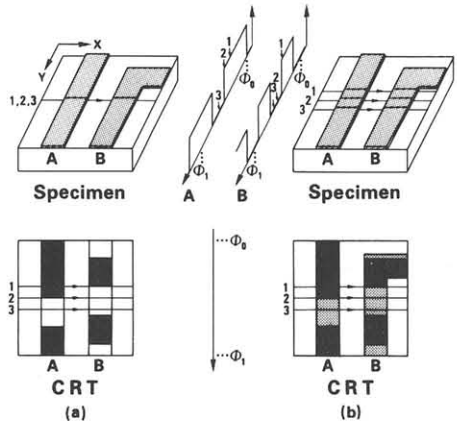

Fig.1 Logic-state mapping mode(a) and phase-stepping image mode(b).

Table I Experimental conditions for stroboscopic observation.

	case A	case B
Beam Accelerating voltage	1 kV	2 kV
Average beam current	.5 pA	2.3 pA
External clock frequency	5.5 MHz	5.5 MHz
Beam pulse width	9 ns	7 ns
Phase step width	5 ns	5 ns
Number of Phase steps	100	100
Recording time	100 s	100 s

Table II Instruction loop.

Adress	Instruction	Code	Clock cycles
8005	MOV A,B	78	4
8006	PCHL	E9	6

Table III Some cardinal time read out from Figs.2 and 3.

	case A	case B
OBFLT "H" "L"	0 ns	0 ns
Data emerges on AD_0 pad	485	489
IBFLT "H" "L"	712	706
Data emerges on data bus	766	756
INSTL "L" "H"	709	709
Data emerges on instruction register	786	777
PCHL instruction "H" "L" on the decoder	735	731
MOV A, B instruction "L" "H" on the decoder	788	793

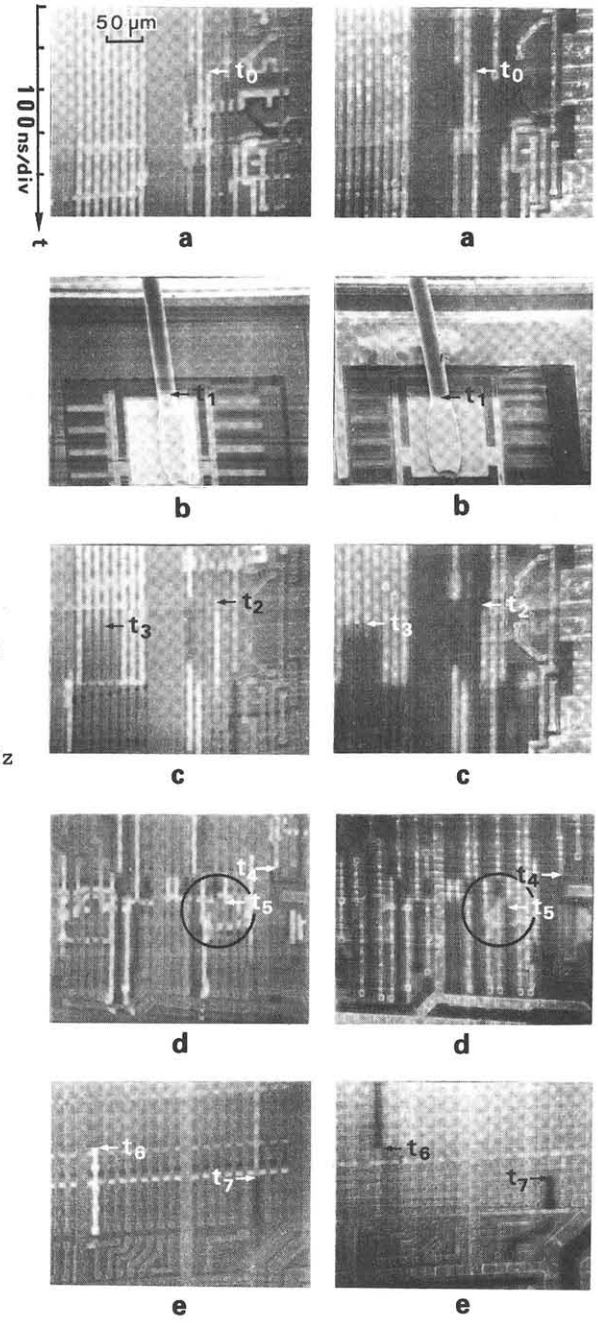

Fig.2 Case A Fig.3 Case B
Stroboscopic micrographs of uP 8085A.
(a) adress/data buffer and data bus at B=1,
(b) adress/data pad at B=2,
(c) adress/data buffer and data bus at B=3,
(d) instruction register at B=3, and
(e) instruction decoder at B=3.