Extended Abstracts of the 15th Conference on Solid State Devices and Materials, Tokyo, 1983, pp. 43-46

A-2-6

Effects of Encapsulation Layers on Planarization of Laser Recrystallized SOI Layers

M.Ohkura, K.Kusukawa, I.Yoshida, M.Miyao, and T.Tokuyama

Central Research Laboratory, Hitachi Ltd.,

Kokubunji, Tokyo 185

Effects of various encapsulation layers in Ar^+ laser recrystallization of poly-Si layers on insulating substrates are investigated. Efforts are focused on planarizing surface roughness caused by the melting procedure down to 50nm. A combination of a Si_3N_4 layer over a SiO_2 layer is found to be most effective for planarization.
Lateral pn diodes fabricated in poly-Si planarized in this way confirm that such layering produces a flat surface with little electrical characteristic scattering.

1. Introduction

Single recrystallization of poly-Si films on insulating substrates by local heating, such as by laser or electron beam irradiation, has recently been attracting great attention as a tool for achieving new device structures. Although electrical characteristics of the layer are found to be comparable to those of bulk silicon[1], surface ripples formed during the melting procedure could cause severe problems when device size is reduced. For example, in fabricating MOSFETs with sub-μm gate lengths, a surface ripple of more than 50nm would result in threshold voltage scattering or source-drain short circuiting.

As a solution to this problem, several researchers have reported the effectiveness of depositing an encapsulation layer on the poly-Si prior to local heating[2,3]. However, experimental conditions have varied widely among these works. Moreover, the role of the layer has yet to be precisely clarified.

The present paper describes systematic investigation of the encapsulation layer effects. Several differnt encapsulation layers were used during Ar^+ laser recrystallization of poly-Si films. Special efforts were focused on planarization of surface ripples down to the critical value of 50nm with a wide range of irradiation conditions. The effectiveness of the encapsulation layer was confirmed by fabrication of diodes that had flat surfaces and little leakage current scattering.

2. Experimental Procedures

A 400nm-thick poly-Si layer was deposited on (100) Si wafers coated with 600nm-thick thermal SiO_2. Encapsulation layers of SiO_2, Si_3N_4, and combinations of both were deposited by the CVD method on the poly-Si layers. Total encapsulation layer thickness was varied from 5nm to 1000nm.

An Ar^+ laser beam focused to about 40μm diameter was used to melt and recrystallize the poly-Si layer. Power and beam scanning speed ranged from 3 to 15W and 1 to 100 cm/s, respectively. The back sides of the samples were

kept at 500°C during irradiation. After laser irradiation, the encapsulation layers were etched off. Surface ripple on the poly-Si was measured by Talystep, and grain growth was observed by TEM and Secco etching.

3. Planarization Effects of Encapsulation Layers

First, the effects of a single encapsulation layer (SiO_2 or Si_3N_4) were investigated.

Irradiation power was normalized to the capless case, considering anti-reflection caused by the encapsulation layers, to make the power absorbed by the poly-Si layers uniform. Normalized power was calculated using a well-known formula[4], and was confirmed by monitoring the poly-Si layer to ensure its melting width remained constant regardless of the encapsulation thickness. In this case, the power level was selected so that the melting width would change rapidly if the power absorbed by the poly-Si changed. For Si_3N_4 encapsulation, the width was found to be constant regardless of encapsulation thicknesses, which guaranteed the calculated values would be correct. In the case of SiO_2 encapsulation, it was found that melting width increased with encapsulation thickness. Thus, power level corrections had to be applied to the calculated value when SiO_2 was used. This increase may be due to the low thermal conductivity of SiO_2.

Surface roughness caused by a single laser scan is shown as a function of cap thickness in Fig.1. The roughness was defined as the height from the lowest level to the highest level on the recrystallized poly-Si surface, as determined from Talystep measurement results. Also shown in the figure are surface photograph of the samples before and after Secco etching. Irradiation power and beam-scanning speed was 10W (normalized to the capless case) and 25cm/s, respectively. These condition correspond to just below those that cause poly-Si layer strip-off in the capless case.

For both SiO_2 and Si_3N_4 encapsulation, surface roughness is seen to fall off rapidly as encapsulation thickness increases. It is reduced to 35nm in the thickness range of 50 to approximately 100nm for both cases. The surface photograph for the 50nm SiO_2 encapsulation case, which is indicated as ② in the figure, shows a flat surface even though the Secco etched surface shows grain growth in the recrystallized poly-Si.

However, above a certain thickness, strip-off or void formation occurs. In the case of SiO_2 encapsulation, strip off of both poly-Si and SiO_2 occurs if the layer thickness exceeds 500nm. On the other hand, in the case of Si_3N_4 encapsulation, tiny voids (approximately 5μm in diameter) form before strip-off occurs, as shown in photograph ③. Such void formation is thought to be due to the concentration of stress induced by movement of the molten Si.

The results indicate that, a SiO_2 encapsulation layer is soft enough to absorb surface motion of molten poly-Si, but it is also so soft enough to be easily stripped off accompanied by molten poly-Si. On the other hand, a Si_3N_4 encapsulation layer is too stiff to absorb surface motion of molten poly-Si leading to void formation and cracking.

From Fig.1, a wide range of cap thickness seems to be applicable. However, in overlapped irradiation, in which the laser beam was stepped 80% of the melting width each successive scan, the

encapsulation layer thickness window was found to narrowed considerably, perhaps due to its thermal history. In the case of SiO_2 encapsulation, strip-off occurred even for optimum irradiation by a single scan. At the same time, the phenomenon was found to be unstable, so that strip-off occurs erratically. On the other hand, crack formation in the poly-Si layer occurred in the case of Si_3N_4, and no significant optimization thickness was obtained for this material.

From these results, it was thought that a composite encapsulation layer, Si_3N_4 on SiO_2, might prove useful. The underlying SiO_2 would absorb the surface motion, while the overlying Si_3N_4 layer would keep the SiO_2 layer from being stripped off. The results obtained using this encapsulation structure are summarized in Fig.2. As shown in that figure, a flat surface is obtained for a wide range of thicknesses. The range also includes a region where the transmission of laser power is over 90%. Additionaly, in this range the transmission value is insensitive to encapsulation thickness deviation. These means that the irradiated laser power can be effectively absorbed by the poly-Si, and at the same time, irradiation effects are insensitive to process fluctuation. The irradiation power range optimum for melting the poly-Si layer has been remarkably enhanced; for example, 10 to 12W in the capless case becomes 10 to 17W (normalized to the capless case) for Si_3N_4(20nm)/SiO_2(20nm) encapsulation.

On the other hand, the opposite structure, SiO_2 on Si_3N_4 resulted in poor characteristics, as are clear from the above discussions.

4. Lateral P-n Diodes Fabrication

The results were applied to fabrication of lateral pn diodes having a surface roughness of less than 50nm.

Without an encapsulation layer, surface ripple depression caused insufficient melting. As a result, the grain size of the beam overlapping region varied greatly from that of the beam center region. By adopting the above mentioned encapsulation layers, sufficient melting was achieved without causing grain size reduction at the overlapping edge.

After recrystallization of the poly-Si layer, B^+ was implanted (75keV, $8x10^{13}cm^{-2}$) to make the whole layer p-type. Then, phosphorus was partly doped by a conventional diffusion process to form an n^+ region. The junction area was 22.4mmx0.4μm (poly-Si thickness) to allow examination of macroscopic effects caused by grain boundaries in the poly-Si.

The diodes were fabricated with junctions parallel to the laser scanning direction. The existence of grain size deviation perpendicular to the laser scanning direction (or junction) would cause large scattering of electrical properties. If the junction area happens to involve a small grain-size region, it would cause poor characteristics. On the other hand, a junction in a large grain area would have satisfactory characteristics.

Leakage current scattering with and without encapsulation layer is shown in Fig.3. Diodes fabricated with an encapsulated layer showed little leakage current scattering due to the absence of grain size reduction.

5. Conclusions

The role of an encapsulation layer in laser irradiation has been clarified. Using a SiO_2 layer (to prevent surface ripple) covered by Si_3N_4 layer (for protection) was found to be most effective for surface planarization. At the same time the range of irradiation conditions was enhanced. Remarkable improvement in electrical characteristics due to this process was confirmed, assuring that the process will be a powerful tool in future sub-um SOI device fabrication.

References:

1) M.Miyao et al.; Appl.Phys.Lett. 41,59(1982).

2) T.I.Kamins; J.Electrochem.Soc. 128,1824(1981).

3) J.B.Lasky; J.Appl.Phys. 53,9038(1982).

4) M.Born and E.Wolf; 'Principles of Optics' (Pergamon,London,1964)

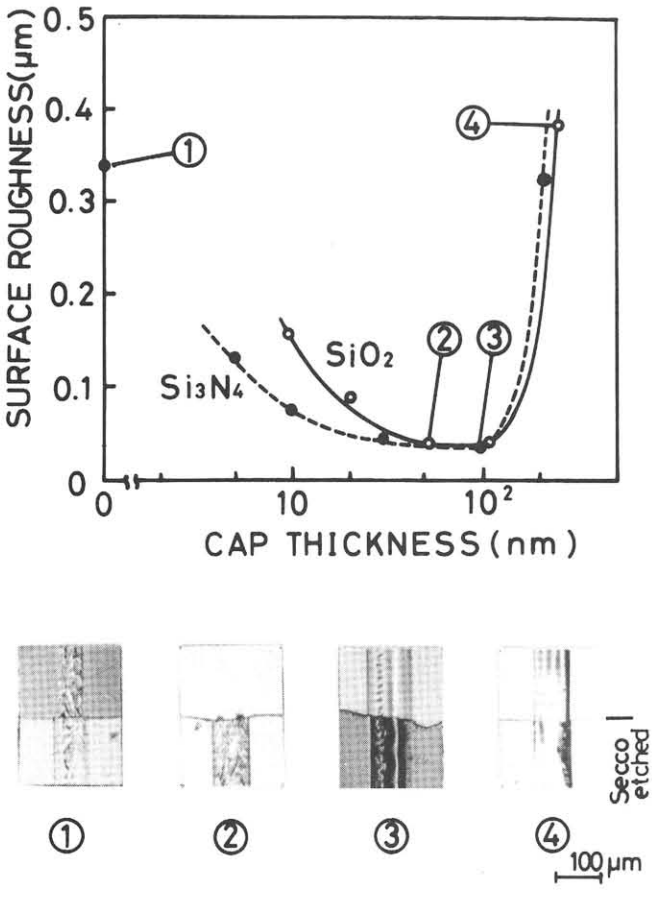

Fig.1 Surface roughness induced by laser irradiation under various encapsulation thicknesses.

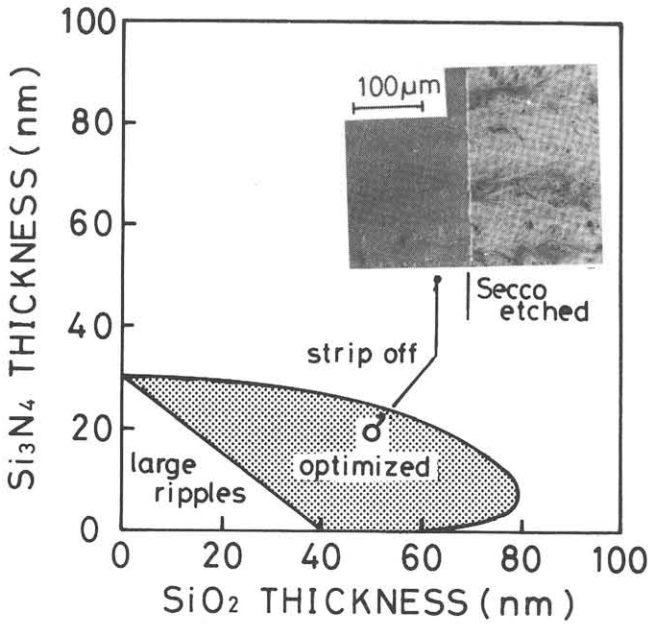

Fig.2 Effects of Si_3N_4/SiO_2 encapsulation layers.

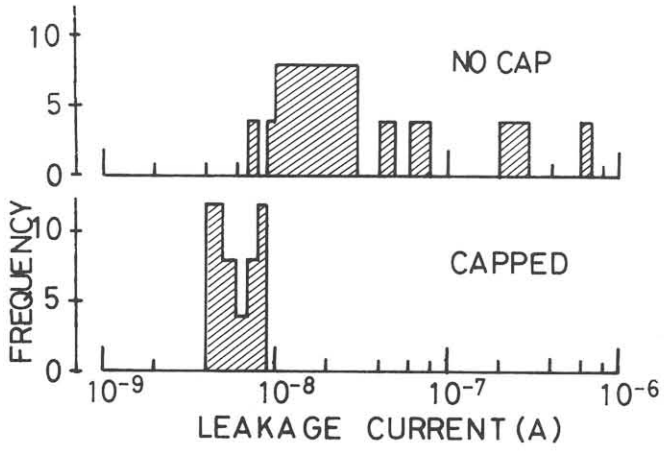

Fig.3 Leakage current scattering in lateral pn diodes with and without encapsulation layers.