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Rapid Annealing of a Polysilicon Stacked Emitter Structure

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The second-duration rapid annealing technique has been applied to an As drive-in process from a stacked poly-Si film for shallow emitter formation. Highly effective dopant activation, especially in the stacked film, can be achieved without deep As diffusion. Remarkable structure changes of the film into single crystals are responsible for dopant activation. Structure change mechanisms are discussed. In addition, high-frequency bipolar transistors with rapid-annealed emitters are discussed to show applicability of the technique.

1. Introduction

The trend toward manufacturing micronized devices prompted an investigation into alternate technologies to alleviate some of the limitations imposed by conventional furnace technology. Recently, high temperature, solid phase annealing over short time periods has been studied intensively as an alternative for obtaining shallower junctions with higher conductivity.[1] Typically, two ranges of intrinsic annealing times are available at present for short term annealing. They are millisecond-duration annealing mainly with laser or electron beam scanning and second-duration annealing mainly with incoherent light lamp or heater irradiation.

From a practical shallow emitter formation point of view, sec-duration rapid-thermal annealing has potential advantages when applied to an As drive-in process from an implanted, stacked poly-Si film. This is because defect-free, shallow, steep junctions with high carrier concentration can be achieved in a compatible manner with reliable contact formation. In this paper, particular features of this emitter formation method are presented.

2. Experimental Prodecures

Typically, 0.16 μm thick, undoped poly-Si films were stacked on (100) Si wafer surfaces using a conventional LPCVD method at 570-630°C. The samples were subsequently implanted with $1.5 \times 10^{16}/cm^2$ As ions at 100 keV. Rapid annealing treatments were simply performed in dry N_2 by rapidly inserting or pulling-out the wafers into or from a furnace. In the present work, a specially designed wafer holder with minimal heat capacity was used so that the wafer temperature was almost able to reach furnace temperature within 4-5 sec after insertion of the wafer. This rapid temperature rise was confirmed by optical thermal monitoring within high temperature regions. Rapid annealing conditions used were mainly in the 1100-1150°C and 15-60 sec range. In comparison, a condition of 950°C, 25 min was employed as the usual standard process.

3. Dopant Activation and Carrier Profiles

Carrier concentration profiles for various annealing conditions were investigated by successive Hall effect and sheet resistivity measurements combined with anodic oxidation layer removal. Typical profiles for isothermal annealing at 1100°C are shown in Fig. 1. The maximum carrier concentration is nearly independent of annealing time and determined by annealing temperature. On the other hand, the junction depth varys

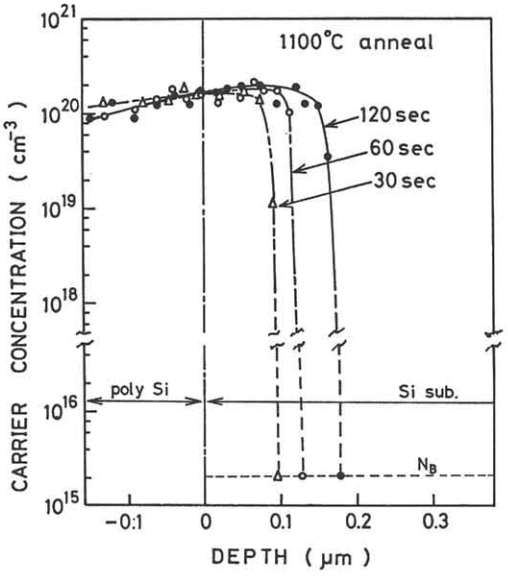

Fig. 1 Carrier concentration profiles for isothermal annealing at 1100°C.

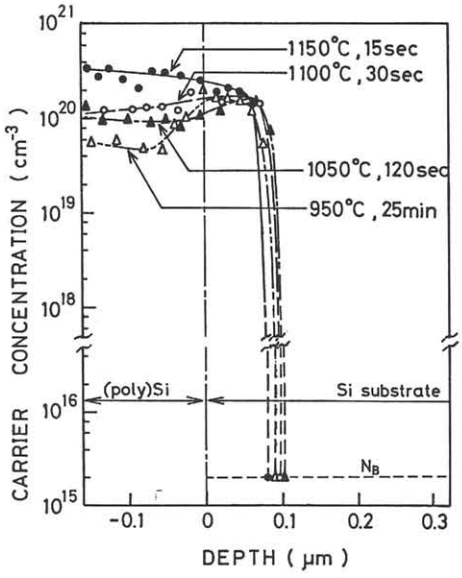

Fig. 2 Carrier concentration profiles with nearly the same junction depth obtained under various annealing conditions.

with annealing time in a manner controled by As diffusion in the substrates. These results suggest that sec-duration rapid annealing at high temperatures is a thermally equilibrium process in contrast to m sec-duration annealing.[2)]

From a practical point of view, carrier concentration profiles with nearly the same junction depth of about o.1 μm are compared in Fig. 2 as a function of annealing temperature. In the substrate, As activation increases depending on annealing temperature as a matter of course. A more remarkable feature for high-temperature, rapid annealing is a drastic increase in carrier concentration in the stacked films. In fact, RBS and SIMS measurements of the total As concentration profiles (not shown) revealed that doping efficiency in the films improved up to 50 % for rapid annealing at 1150°C from 10 % for conventional annealing at 950°C.

4. Structural Changes in Stacked Films

The reason for this remarkable carrier concentration increase in the film was studied from a viewpoint of crystalline structure changes. Channeling RBS spectra for typical samples, in Fig. 3(a), clearly show an epitaxial alignment of a rapid-annealed film at 1150°C. In contrast, the spectrum for a conventionally annealed film at 950°C showed little change from that for an unannealed sample. TEM observation of

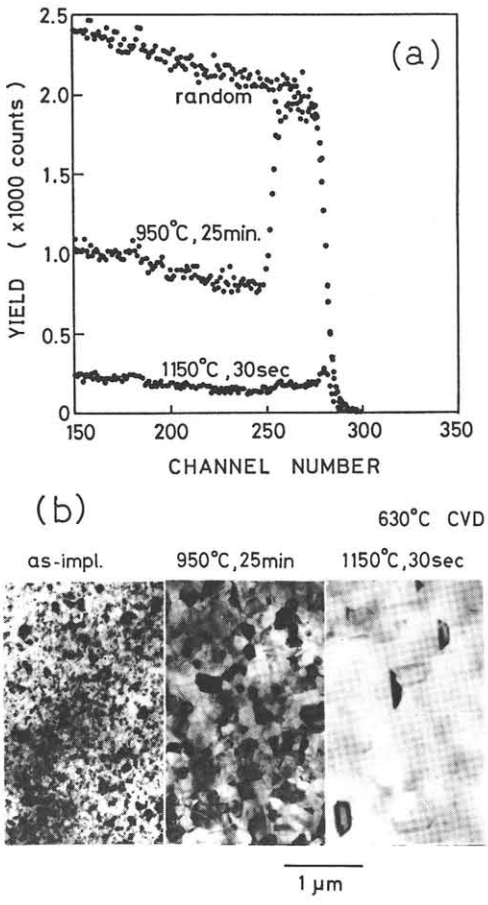

Fig. 3 Structure changes of stacked films investigated by RBS measurements (a) and TEM observations (b).

the same samples,(Fig. 3(b)),indicates that in the rapid annealing case, the poly-crystalline structure vanished and turned into single crystalline structures with many twins. On the other hand, a poly-crystalline structure remained in the conventional annealing case, although obvious grain growth was observed. These results naturally lead to the conclusion that doping efficiency in the stacked layer is determined primarily by the degree of grain growth. In extreme cases, epitaxial alignment with grain boundary disappearance effectively enhances active As incorporation to a level obtainable in single crystals. This is because most inactive As atoms trapped at grain boundaries must be dissolved. In addition, it may be useful to note here that in both cases, no defect was observed in the As driven-in single crystalline substrates.

Epitaxial alignment of undoped poly-Si films have been reported to be induced by annealing at a sufficiently high temperature for a long time.[3] However, the doping enhancement effects are like those known in grain growth phenomena. Therefore, in this case, the epitaxial alignment phenomenon easily occurs in sec-duration annealing. Experiments using TEM, RBS and X-ray diffraction measurements have been conducted to clarify the mechanism of this phenomenon. The results obtained are as follows and schematically depicted in Fig.4.

Initial deposited films consist of fine grains with weak preferred orientations of (110) or (111) depending on deposition temperature. These grains grow slightly during As implantation. In the first annealing stage, subsequent grain growth takes place until average grain size becoms comparable to film thickness. Consequently, the grains become columnar shaped. During this stage, no obvious enhancement of preferred orientation is observed. Therefore, in this primary recrystallization and grain growth stage, reduction in grain boundary energy is thought to provide the dominant driving force. After a latent period, the

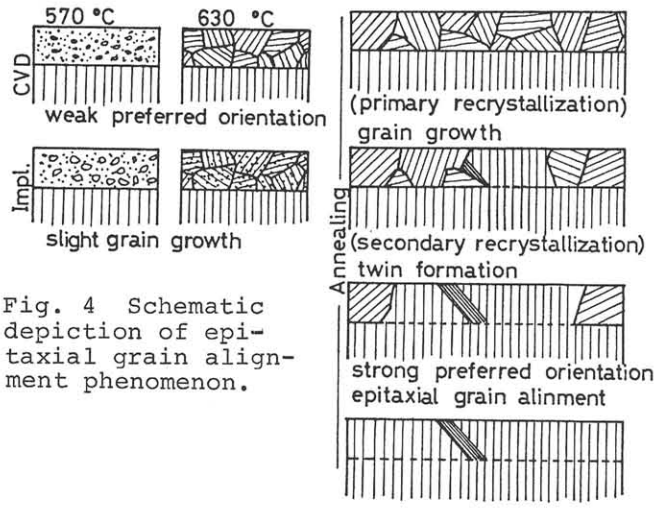

Fig. 4 Schematic depiction of epitaxial grain alignment phenomenon.

second annealing stage starts.

In the second stage, some grains at random positions epitaxially align and subsequently grow laterally to consume the remaining unaligned grains. The initiation of this stage coincides with that of the secondary recrystallization of poly-Si films on silicon dioxide. This implies that reduction in interface energy between deposited film and the substrates is the dominant driving force, namely, pronounced effects of the substrates on the recrystallization do appear. The apparent activation energy estimated for the present epitaxial alignment is 5-6 eV which shows fairly good agreement with that for Si self-diffusion.[4] This result in conjunction with the fact that many twin lamellae lying on (111) planes remain in the epitaxially aligned films suggest the boundary migration mechanism. Thus, it became apparent that epitaxial grain alignment occurs mainly as a secondary recrystallization.

5. Device Fabrication

Discrete npn transistors have been fabricated using standard ion implantation and poly-Si deposition processes combined with the rapid annealing. In this fabrication, activation of implanted B and drive-in of As from an implanted, stacked poly-Si film was simultaneously performed by one rapid annealing treatment in order to achieve a shallow emitter and a narrow base. It was confirmed that the competitive relation

between As and B diffusion at a high temperature did not differ so much from that at lower temperatures. It was also found possible to avoid emitter push-out or suck-in effects under appropriate implantation and annealing conditions.

Typical grounded emitter output characteristics of rapid-annealed transistors are compared with those of conventionally annealed transistors in Fig. 5. Somewhat higher current gain is observed for the rapid-annealed transistor. The increase in emitter carrier concentration is thought to contribute to this to some extent. The emitter-base and collector-base junction I-V characteristics of the rapid-annealed transistor are not at all inferior to those of the conventionally annealed transistor. Thus, rapid heating and cooling processes do not degrade the SiO_2/Si interface in contrast to m sec annealing. In addition, cut-off frequencies of 9-10 GHz were achieved with reasonable breakdown voltages as shown in Fig. 6. These results shed light on the feasibility of further improvement in making shallow emitters having large Gummel numbers.

6. Conclusion

The second-duration, rapid-thermal annealing technique has been successfully applied to an As drive-in process for a shallow poly-Si stacked emitter formation. Transformation of stacked poly-Si films into single crystals during high-temperature, rapid annealing was found to give highly effective dopant activation. The applicability of this technique to high-frequency bipolar transistors was confirmed through device fabrication. These results lead to the conclusion that the rapid annealing technique provides a promissing means for further developing device processing.

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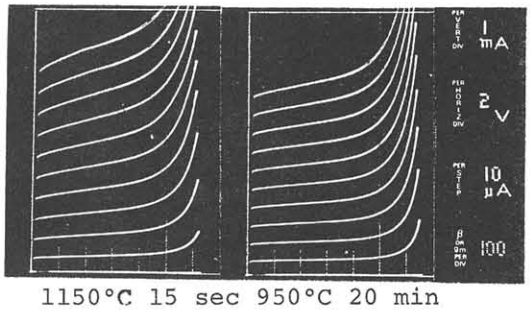

1150°C 15 sec 950°C 20 min

Fig. 5 Grounded emitter output characteristics of a rapid-annealed transistor and a conventionally annealed transistor. Their emitter junction depth and base width were estimated to be ~120 nm and ~140 nm respectively.

Values of f_T (at Ic=30 m A) and τ_i are listed below.

	f_T(GHz)	τ_i(ps)
1150°C, 15 sec	9.0	12.5
950°C, 20 min	8.2	12.5

Process conditions

Substrate:	1 ohm-cm, 1.5 µm epitaxial layer	
B impl.	:	25 keV, $3.5\times10^{13}/cm^2$ through 50 nm SiO_2
Poly-Si	:	160 nm, LPCVD
As impl.	:	100 keV, $1.5\times10^{16}/cm^2$

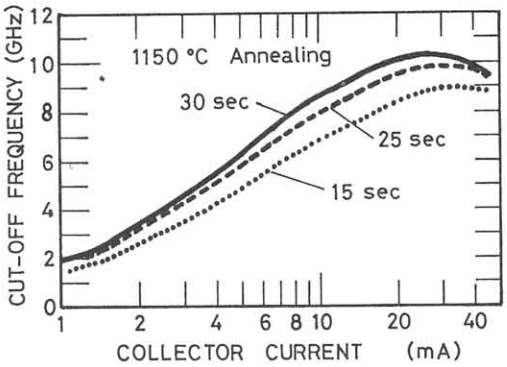

Fig. 6 f_T VS. Ic characteristics for some transistors fabricated using rapid-thermal annealing.

Values of τ_i and breakdown voltages are listed below.

	τ_i(ps)	BVebo(V) (at 10µA)	BVceo(V) (at 100µA)
15 sec	12.5	4.6	28
25 sec	12.0	5.0	16
30 sec	11.0	4.6	9.5

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