RECENT PROGRESS IN SOI TECHNOLOGIES

Hon Wai Lam

Texas Instruments Incorporated

MS 944, P. O. Box 225621

Dallas, Texas 75265

ABSTRACT

Silicon-on-Insulator (SOI) technologies are becoming more important as CMOS becomes the preferred technology for VLSI. The progress of the three most actively researched SOI technologies, beam-recrystallized SOI, implanted buried oxide and Full Isolation by Porous Oxidized Silicon will be summarized in this paper. The thin film SOI transistor concept extends the realm of monolithic integrated circuit to the vertical dimension and one example of such structures, stacked CMOS, will be discussed.

INTRODUCTION

Silicon-on-Insulator (SOI) refers to a generic class of materials where a crystalline silicon film is supported on an insulating substrate. Silicon-on-Sapphire (SOS) is a classic example of an SOI technology. Recently, there are several new approaches for the implementation of SOI. They are, namely, beam-recrystallized SOI [1-4], implanted buried oxide (also known as SIMOX for Separation by IMplanted OXygen) [5-7], FIPOS (which stands for Full Isolation by Porous Oxidized Silicon) [8], epitaxial overgrowth [9] and graphoepitaxy [10]. The efforts on epitaxial overgrowth and grapoepitaxy have been relatively small due to some fundemental problems that are encountered with these two processes. The efforts devoted to the first three new approaches, however, have grown significantly in the last three years.

Although there are increasing interest in the application of SOI in large area display [11] and high voltage [12] applications, the rapid growth in the interest in the new SOI technologies arises from the fact that CMOS is becoming more important in VLSI, primarily for power consumption and heat dissipation considerations. A CMOS/SOI technology is superior to a bulk CMOS technology because it eliminates latch-up, increases packing density and increases circuit speed due to reduced parasitic capacitance and reduced chip size.

When one is freed from the constraints imposed by device fabrication in a bulk wafer, the thin-film SOI transistor approach, especially that of a deposited silicon on dielectric material, allows one to contemplate a three-dimensional circuit, which may extend the performance and packing density of integrated circuits beyond VLSI. A prime example of a three-dimensional device structure is stacked CMOS [13].

In this review paper, we will explore the development of SOI technologies to date, with primary emphasis on those developments that address applications in VLSI.

BEAM-RECRYSTALLIZED SOI

Beam-recrystallized SOI, a thin film zone melting process, has progressed from the use of an unseeded approach [1,2] to a seeded approach [3], from using a scanning cw argon ion laser beam to a graphite strip-heater [4], which has resulted in the ability to process a large wafer in a short time. All the different recrystallization approaches start with the deposition of a polysilicon film on top of a dielectric layer, which, in the case of most VLSI applications, is an oxide layer thermally grown on top of a single crystal silicon wafer. In the case where seeding is used, part of the underlying silicon wafer is exposed so that it is in contact with the deposited polysilicon. A heat source is then scanned across the surface of the polysilicon such that the area under the illumination is melted. As the heat source is scanned away, the molten silicon freezes and crystallizes, resulting in the formation of large grains. In the case where a seed is used, single crystal films are formed.

These single crystal films, however, are not free of defects. Sub-boundaries or small angle grain boundaries are commonly found in these films [14]. It is commonly believed that the sub-boundaries are formed when the moving solidification front becomes

unstable due to constitutional supercooling, which is a result of saturation of impurities in the molten silicon. The unstable solidification front will result in dendritic growth into the melt. When these dendrites eventually merge, the sub-boundaries are formed. Electron channeling patterns were used to investigate the degree of misorientation across the sub-boundaries, and it was found that the misorientation across one sub-boundaries was less than 0.3 degree [14]. It was also possible to image the individual dislocations that made up the sub-boundaries using transmission electron microscopy. Devices that are fabricated in these recrystallized films exhibit characteristics that are comparable to those observed in bulk silicon, with the floating body and the back interface exerting their usual influences [15,16]. Kinks in the I-V characteristics of an MOSFET device are usually observed and is believed to be caused by the charging of the floating body due to majority carrier injection resulting from impact ionization at the drain junction. The back interface charges in the recrystallized SOI structure have been measured and the density is typically on the order of 5 to 10 X 10^{11} per cm^2. Hence, a boron ion implantation on the order of 1 to 3 X 10^{12} per cm^2 aimed at the back interface is normally sufficient to suppress the leakage current.

One additional advantage of the new SOI structure over SOS is the ability to apply a relatively small bias at the substrate to affect the leakage at the back interface due to a relatively thin oxide layer that is used as the dielectric layer [16,17,18]. This terminal will provide an added dimension for controlling the device characteristics as is evidence in References 16 17, and 18.

It was observed that the interface trapping density in the sub-boundaries is typically in the range of 5 to 10 X 10^{11} per cm^2 [19]. It was found that the net effects of the traps on the device characteristics are a shift in the expected threshold voltage and a higher effective mobility in the linear region of the device [20]. Bipolar devices have also been fabricated in the recrystallized material and a typical lifetime on the order of 1 micro-second has been measured [21].

The heat source used in the recrystallization process has progressed from a scanning cw argon ion laser [3] to the graphite heater [4] and more recently to a scanning lamp system. Both a scanned tungsten lamp [22,23] and a scanned mercury arc-lamp have been used [24]. Regardless of the heat source used, the resulting crystalline structures are similar to those discussed earlier. However, the controllability of the process is greatly improved, primarily due to an increased in the ability to control the uniformity of the incident radiation on the surface of the wafer. Nonetheless, large area single crystal SOI materials have been successfully crystallized using the different heat sources.

Although significant progress has been made in this field, there are problems that remained to be solved. The wafer is usually severely stressed when it goes through the recrystallization process, resulting, in most instances, the formation of slips in the underlying silicon wafer. We have observed that these wafers have a higher tendency to become slightly deformed during subsequent device processing, resulting in difficulties in pattern alignment in photolithography. However, more careful attention to the reduction of thermal gradients, both in space and in time, can significantly reduce this problem.

No doubt that the characteristics of devices fabricated in this material have shown significant promise, the ability of this material to support a VLSI class circuit has yet to be proven. Presently, the research efforts are divided into two groups: one to determine if VLSI class circuits can be fabricated in the presence of the sub-boundaries, and the other to develop means to eliminate the sub-boundaries.

IMPLANTED BURIED OXIDE

The implanted buried oxide SOI material is formed when a very high fluence of oxygen ions (on the order of 1 to 2 X 10^{18} per cm^2) is implanted beneath the surface of a silicon wafer. The implantation conditions are chosen such that the a continuous oxide layer is formed, separating the substrate from the surface. The crystallinity of the surface is maintained during the implantation by a self-annealing process, which is enhanced by elevating the temperature of the wafer during the implantation [6].

The typical acceleration energy used is 150 keV for O+, with a projected range of 0.37 micron and a projected standard deviation of 0.01 micron. These conditions were first reported by Izumi et al. [5]. With a fluence of 2 X $10^{18}/cm^2$, a 0.5 micron thick buried oxide layer is formed, leaving a surface silicon layer of about 0.12 micron [25]. Molecular oxygen ions have also been implanted at 300 keV, thereby reducing the fluence and hence the implant time by one half [6]. The results obtained using molecular oxygen are the same as those obtained using atomic oxygen ions at half the nominal implantation energy.

The feasibility of performing the implantation of atomic oxygen ions at 80 keV has also been demonstrated [26]. It was found that at the lower implantation energy, a lower dose of 1.5 X $10^{18}/cm^2$ is required to obtain stoichiometric silicon dioxide. The thickness of the surface silicon layer is accordingly reduced to about 50 nm. Although this

surface layer is thin, its crystalline quality is good enough to support epitaxial growth.

The implanted wafers are usually treated with a post implantation thermal anneal which serves two purposes. A high temperature anneal allows solid phase epitaxial regrowth from the crystalline surface region down towards the highly damaged region above the buried oxide layer. A high temperature process is also required to complete the out diffusion of the implanted oxygen towards the silicon/silicon dioxide interface and to complete the chemical reaction for the formation of the silicon dioxide. Although different temperatures have been tried, 1150°C seems to be necessary to form a stable silicon dioxide layer. Solid phase regrowth has been observed at temperatures as low as 750°C [6], but the crystalline quality of the top silicon layer improves as the anneal temperature is increased.

Between the buried silicon dioxide layer and the regrown top silicon layer, there is always a highly defective layer of silicon where the oxygen concentration is very high [27]. It is believed that a high oxygen concentration in the form of oxygen precipitates in that region inhibits the solid phase epitaxial process, resulting in the random nucleation of silicon into a polycrystalline or a highly defective state.

A buried channel 15-stage CMOS ring oscillator with 0.5 μm channel length has been fabricated [28]. A delay time of 139 ps at a supply voltage of 3.5 V has been measured. Fabrication of two CMOS LSI circuits on the buried oxide material has also been reported [29]. A 1 kbit CMOS static random access memory (sRAM) circuit has been fabricated with 1.5 μm effective channel length with a chip-select access time of 12 ns at a 5 V supply voltage. A phase-locked-loop circuit, which consisted of about 400 gates, operated at a maximum frequency of 420 MHz.

Materials and process developments not withstanding, the most important element required for the successful implementation of this technology is the development of a high beam current ion implantation machine. Presently, the state of the art equipment can deliver a beam current of 5 to 10 mA of oxygen at a maximum energy of 160 keV. For the implanted buried oxide process to be successful, an implantation machine that can deliver at least 100 mA at 150 keV is required. However, this machine is not expected to be available in the near future, casting doubt on the production viability of this process within the next two years.

FULL ISOLATION BY POROUS OXIDIZED SILICON (FIPOS)

In the FIPOS process [8], selected surface areas of a p-type wafer are converted to n-type and covered with a silicon nitride layer. The wafer is then immersed in an HF anodization solution where the wafer serves as the anode and a platinum electrode is used as the cathode. The subsequent anodization process converts the exposed surface p-type regions into porous silicon while leaving the surface n-type regions intact. Done properly, the anodization will proceed around and will undercut the n-type regions. A high temperature oxidation step follows where the porous silicon layer is oxidized rapidly, resulting in complete dielectric isolation of the n-type islands, which will form the body regions for subsequent device fabrication.

Because of the isotropic nature of the anodization process, the thickness of the porous layer is directly proportional to the width by which the porous region undercuts the islands. Hence, for full dielectric isolation of a 10 microns wide island, a 7 to 8 microns thick porous layer is required. We have observed that when the porous layer thickness exceeds 8 microns, the warpage in the wafer after oxidation becomes excessive. This limitation on the porous layer thickness also restricts the maximum width of the silicon islands to about 10 microns. One approach to circumvent this limitation is to divide a wide island into several islands [30].

It was found that [31,32] the porous silicon layer after anodization is monocrystalline, with the same orientation as the host crystal from which the porous layer is formed. This has been verified by both electron and x-ray diffraction. This fact has been exploited by Konaka et al. [33] in developing an alternate approach to the FIPOS process. In their approach, an unpatterned p-tpye wafer is uniformly anodized. An epitaxial layer is then grown on the porous layer using molecular beam epitaxy. The epitaxial layer can then be patterned and etched. The then exposed regions of the porous silicon layer can be oxidized. The porous silicon regions beneath the epitaxial islands will also be oxidized due to rapid diffusion through the porous layer. This approach reduces, to a certain extend, the limitations on the size of the islands and on the thickness of the porous layer due to warpage. Molecular beam epitaxial was used because any high temperature process, such as a conventional CVD epitaxial growth, will cause an unoxidized porous layer to collapse, restricting the oxidation through the porous layer.

Another approach that may overcome the problems mentioned earlier is being investigated [34]. This new approach relies on the electrical breakdown between an HF solution and a heavily doped n-type region (on the order of 1×10^{17} per cm^2 or higher). Because of this sharp breakdown characteristic, which is dependent on the impurity level, the

anodization process is self-limiting on layers of different doping concentration. With this approach, Holmstrom and Chi [34] were able to dielectrically isolate lightly doped, n-type silicon islands as wide as 40 microns with a heavily doped, n-type porous layer that was only 5 to 6 microns thick. They claimed that it would be possible to isolate islands up to 300 microns wide.

Very impressive circuit results, nonetheless, have been achieved in the conventional FIPOS material. A 1.3 Kgates gate array have been fabricated with good yield and 20% higher speed compared to conventional bulk CMOS [8]. A 16 K-bit sRAM have also been fabricated with a 2 micron CMOS/SOI technology resulted in a 35 nsec access time with a 250 mW power dissipation at a 300 nsec cycle time [30].

If the problems of warpage and limited island size are solved and if the anodization and oxidation process prove to be uniform and reproducible, the FIPOS process can be an attractive SOI process.

Three Dimensional Integrated Circuit (3DIC)

In an initial study of stacked CMOS [13], one form of 3DIC, an n-channel thin film SOI device is stacked on top of, and shares the same gate with a bulk, p-channel device. This structure possesses the same advantages of CMOS/SOI; in addition, it promises an even higher packing density and a higher level of integration.

The p-channel device is stacked on top of a bulk n-channel device in more recent approaches [35,36]. In this case, the stacked device is laser-recrystallized. Isolated stacked CMOS inverters have also been demonstrated [37].

Recently, a stacked-CMOS-based sRAM cell have been demonstrated [38]. This circuit was fabricated with a modified 2-poly nMOS process, where the second polysilicon layer constituted the body of the stacked p-channel transistor. These memory cells have been exercised through the write and read cycles with external signal generators while the output of the memory cells is buffered by stacked-CMOS-based preamplifiers.

Although the relatively low performance of the stacked p-channel device is excluding the current stacked CMOS structure from high speed logic application, the demonstration of the stacked CMOS sRAM cell has paved the way for the application of stacked CMOS to high density memory applications where the improved packing density will give the stacked structure a distinctive advantage. However, a lot of work needs to be done to perfect the structure. The challenges in achieving this end are in the development of a p-channel device with acceptable characteristics, the development of a stacked device process that is compatible with the host bulk processing, and the development of self-alignment schemes for the stacked device.

SUMMARY

The increasing prevalence of CMOS has made SOI an increasingly attractive material for VLSI. Three approaches, recrystallized SOI, implanted buried oxide and FIPOS are being pursued very actively for this application. The progress to date has been discussed. Stacked CMOS structures are also gaining attention as a technology that may have longer term impacts.

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