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Lateral Epitaxy of Si Films Deposited in a UHV Ambient by Electron Beam Annealing

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Laterally seeded recrystallization of silicon layer evaporated in an ultra high vacuum has been studied experimentally by a scanning electron beam annealing. Silicon layer on the seed area was grown epitaxially during the evaporation. Silicon layer of above 1 μm thickness was successfully recrystallized, resulting in reproducible lateral epitaxy of 40 μm in length. A pseudo-line shaped electron beam formed by high frequency oscillation enabled dimensional enlargement of lateral epitaxial growth up to 200 μm in length. Crystalline properties were characterized by Rutherford back-scattering measurement and electron channeling observation.

1. Introduction

Growth of silicon films on insulating materials (SOI) is key technology for realizing three dimensional devices. Lateral seeded epitaxy technique has been believed to be advantageous in controlling the location of single crystalline area by lithographically determining seed position. Although many workers have concentrated their efforts on this technique[1-5], lateral propagation length of the epitaxial layer is reported to be not yet satisfactory, typically a few tens of micrometers. Crystalline quality of the epitaxial layer has not yet been characterized sufficiently.

Lateral epitaxy is ruled by several parameters, such as impurity segregation of H_2, N_2 and O_2 at growth front[5], difference in heat dissipation between seed area and SOI area, thermal gradient profile and stress distribution in the wafer. Most of the experiments reported had employed CVD polycrystalline silicon layers. Impurities in the silicon layer are included during CVD process and/or adsorbed during the beam annealing. The experiments reported need both vertical and lateral epitaxy, because silicon layer on the seed area is polycrystalline, as shown in Fig. 1 (a), which can be realized in a relatively narrow window of annealing condition for adequate melting of both seed and SOI areas.

This paper describes experimental results using high purity silicon evaporation and electron beam (EB) annealing, both of which were carried out under ultra high vacuum (UHV) condition. The margin of annealing condition was expanded by using the sample with epitaxially grown silicon layer on the seed area, which does not need complete melting of the silicon in the seed area. Pseudo-line shaped electron beam annealing was examined to improve thermal gradient profile and to enlarge the epitaxial silicon area.

2. Experiments

Silicon wafers of (100) orientation with 200 nm thick thermal oxide layer were chemically etched to delineate stripe patterns with 6 μm spacing and line width ranging from 6 to 200 μm. The wafers were rinsed in mixed solution of HCl, H_2O_2 and H_2O and then in deionized water to eliminate carbon contamination and to form protective oxide layer of ~1 nm thickness. The wafers were quickly loaded into an UHV silicon deposition chamber through a load lock mechanism. The chamber was evacuated to 2×10^{-10} Torr with cryo-pump, ion pump and titanium sublimation pump. Liquid nitrogen cooled shrouds were located to surround the wafer and a silicon evaporation souce. By heating the wafer up to 800 °C using tungsten resistance heater, the protective oxide layer was sublimated and atomically cleaned surface appeared. Successively, silicon layers of 0.5 ~ 2.0 μm thickness were evaporated from E-gun source at substrate temperature of 370 ~ 600 °C. The pressure during the evaporation was kept below

5×10^{-9} Torr. Silicon deposition rate was 3nm/min. At substrate temperature above 370°C, silicon was epitaxially deposited onto seed area in this experiment. Amorphous and polycrystalline silicon were deposited on SiO_2 layer at substrate temperature below and above ~ 500°C, respectively. The cross sectional structure of the sample is shown in Fig. 1 (b).

Electron beam annealing was carried out by a scanning electron beam of 10 kV acceleration volatage. The scanning for x-direction was in the range of 10 ~ 150 cm/s. The scan line displacement for y-direction was 10 μm/step. Beam current and beam diameter were 1.8 ~ 3.6 mA and 100 μm, respectively. The wafer was heated at 500 °C during the annealing by a tungsten radiation heating system. Annealing chamber was evacuated to 1×10^{-8} Torr during annealing with oil-free pumps. Some of the wafers were annealed by a pseudo-line shaped electron beam[6], which was made by adding high frequency oscillation perpendicularly to the x-direction.

Grain boundary was observed by a Normarski optical microscope in the sample etched in mixed solution of HNO_3, HF and CH_3COOH. The crystalline properties of the annealed silicon layers were characterized by Rutherford backscattering and channeling of 350 keV protons and electron channeling pattern observation.

3. Results and Discussion

3.1) Lateral epitaxy by a conventional EB annealing

The important problem in establishing lateral epitaxy technology is how to smoothly recrystallize silicon layers on both the seed area and SiO_2 layer. Beam power needed for adequate melting of silicon layers on both regions is significantly different; the former is larger than the latter, because of the difference in heat dissipation into the silicon substrate. In order to moderate this difference, we have examined the following two; one is increase of lateral heat dissipation by using thick silicon layer and the other is decrease of beam power for melting seed area by using epitaxial silicon layer in the seed area.

Thicker silicon layer proved to have wider margin in melting the above two regions. Sample with more than or equal to 1 μm thick silicon layer were melted smoothly, whereas those with 0.5 μm thick silicon layer on SiO_2 was vaporized when that of the

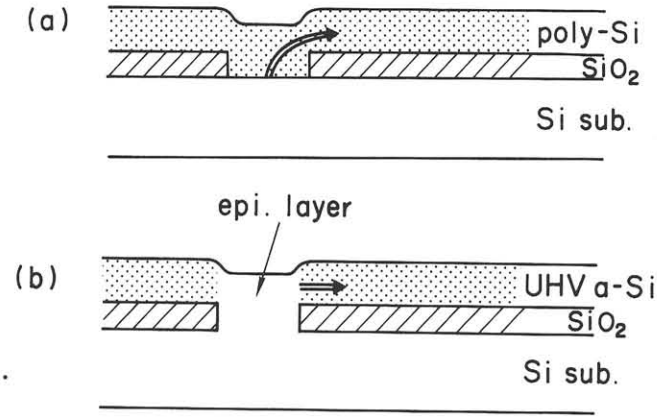

Fig. 1 (a) conventional sample structure, which needs both vertical and lateral epitaxy.
(b) sample structure used in this expriment, which has epitaxial silicon on seed area.

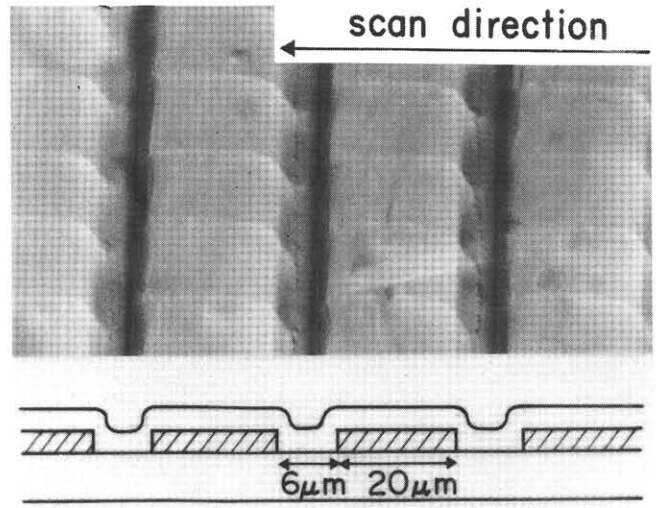

Fig. 2 Optical micrograph of completely epitaxially grown sample.

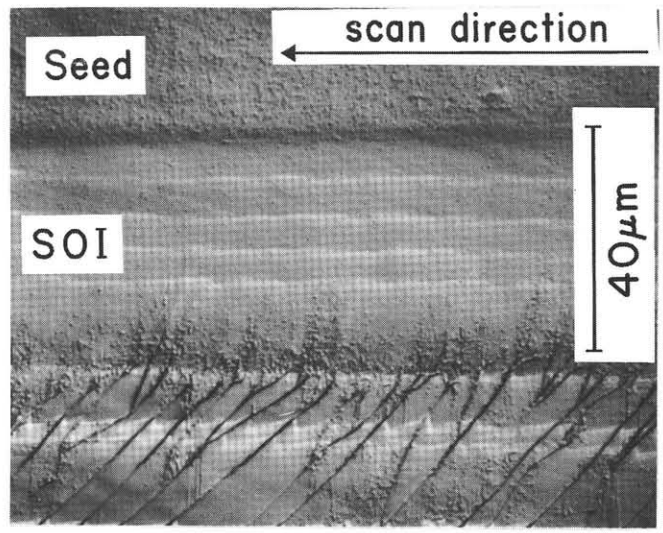

Fig.3 Optical micrograph of annealed sample etched in mixed solution of HNO_3, HF and CH_3COOH.

seed region was melted. This is because lateral heat dissipation within the silicon layer on SiO_2 is more effective in thicker silicon layer. For the choise of starting material, polycrystalline silicon was superior to amorphous silicon, because of the difference in thermal conductivity. Cap layer of 0.2 μm thick SiO_2 layer proved to have heat accumuration effect, which rather prevent to expand the annealing margin.

Fig. 2 shows an example of completely epitaxially grown sample with the SiO_2 stripe of 20 μm width. The surface is considerably smooth and no grain boundary is observed. The complete epitaxy is reproducibly obtained in the wide range of annealing conditions examined. This is because complete melting of the silicon layers in the seed area is not needed for lateral epitaxy.

Fig. 3 shows a typical example of lateral epitaxy by annealing with electron beam scanned parallel to the stripe pattern. The thickness of the silicon layer was 1.5 μm. Etch pit density in the lateral epitaxial region is fairly low, but it abruptly increases at the region ~30 μm apart from the seed edge. Grain boundaries originate from the position 40 μm apart from the seed edge, where etch pit density is significantly high. Electron beam scanning perpendicularly to stripe pattern leaded to almost the same crystal growth. This phenomenon may be due to microscopic non-uniformity of thermal gradient and/or stress distribution.

3.2) Lateral epitaxy by pseudo-line beam annealing

In order to moderate thermal gradient in the annealing area, pseudo-line shaped beam was examined. Deflection by sine wave of 3 MHz frequency and 30 V peak to peak amplitude leaded to 200 μm line length. Because the dwell time of the beam is estimated to be less than 80 ns, the beam intensity variation within the oscillation period can be neglected from viewpoint of temperature variation at the sample surface. The scanning rate was 10 mm/s and the scan line displacement was 100 μm/step.

As shown in Fig. 4, large area lateral epitaxy is obtained. The epitaxially grown area has tendency to be triangular shape, which is due to grain boundary generation at the edge of the line beam in the seed region. The epitaxially grown area has dimension of ~150 μm in width and ~120 μm in length. The etch pit is scarecely seen in the lateral epitaxial region. An example of 200 μm long bridging of epitaxy is shown in the middle of Fig. 5.

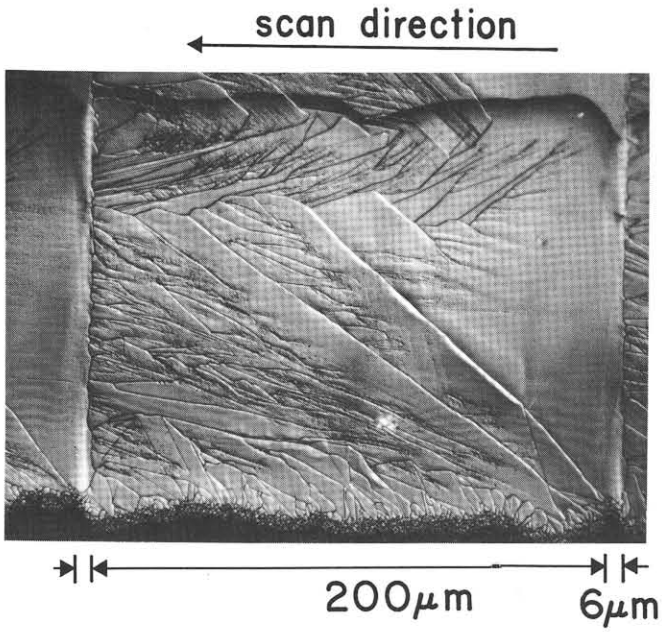

Fig. 4 Optical micrograph of sample annealed by pseudo-line shaped electron beam.

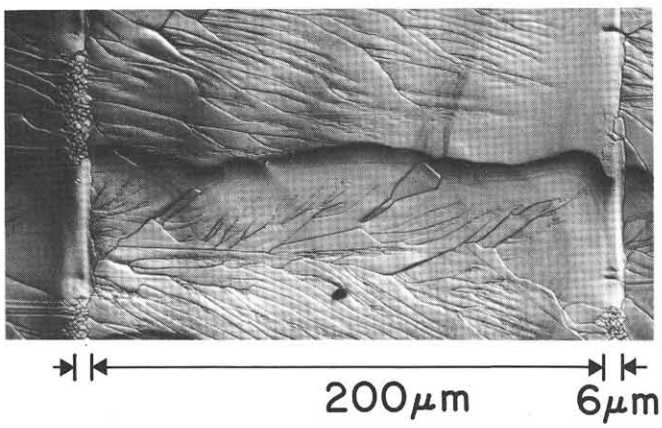

Fig. 5 Optical micrograph of sample annealed by pseudo-line shaped electron beam. complete overbridging of lateral epitaxy is seen in the middle.

3.3) Evaluation of epitaxial layer

Fig. 6 shows backscattering and channeling spectra from the completely epitaxially grown sample as is shown in Fig. 2. About 77 % of the analyzed area corresponds to the SOI area. Normalized minimum yield (χ_{min}) is 0.24 and uniformly distributed in depth scale throughout the SOI layer. Comparing with χ_{min} of the (100) bulk silicon, there exist high density crystalline disorders, comparable to that of SOS film at silicon/

sapphire interface. There, however, is a possibility of χ_{min} increase by crystal bending[7], which may result from remaining stress in the SOI layer. Electron channeling pattern observation proved that lateral epitaxial layer has (100) orientation, which is the same as that of the silicon substrate, as seen in Fig. 7 (A). Texture structure appears in the transition region from which subgrain boundaries originate, as seen in Fig. 7 (B).

4. Summary

Lateral epitaxy of silicon layer on SiO_2 from lithographically determined seed area was studied by using a scanning electron beam annealing. The silicon deposition and the electron beam annealing were carried out in an UHV ambient in order to prevent impurity incorporation. Annealing margin for melting silicon layers on the seed area and SiO_2 was expanded by using epitaxially grown silicon on the seed area and silicon layer thicker than or equal to 1 μm.

Lateral epitaxy of 40 μm long was reproducibly performed by the conventional scanning electron beam annealing. A pseudo-line shaped electron beam annealing enabled large area lateral epitaxy of 120 μm long and 150 μm wide, which is considered to be due to improved thermal gradient profile at the annealed sample surface. Electron channeling pattern observation verified crystallographic orientation of the lateral epitaxial layer is the same as that of the substrate. Crystalline quality characterized by Rutherford backscattering proved to be relatively poor, which is remained to further improvemnt of lateral epitaxy technique.

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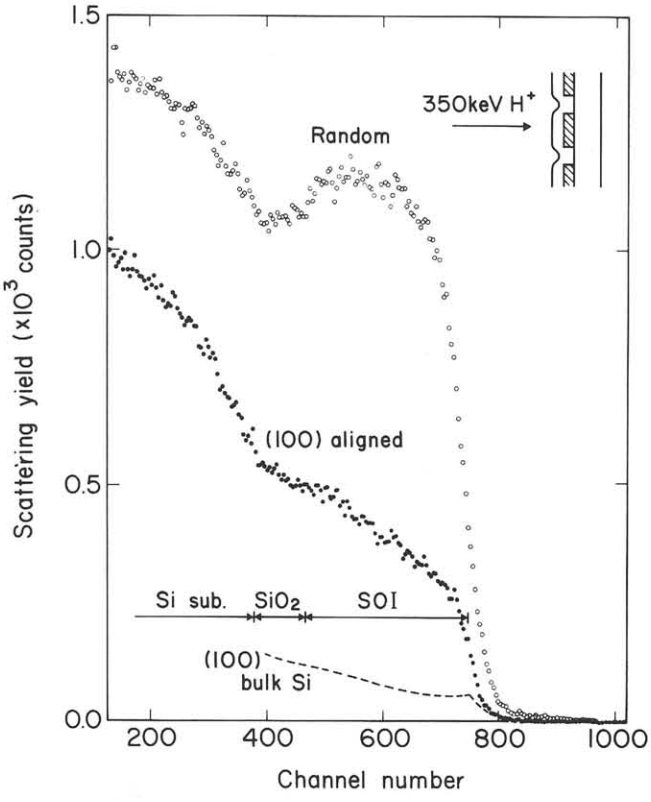

Fig. 6 Rutherford backscattering and channeling spectra from the sample shown in Fig. 2.

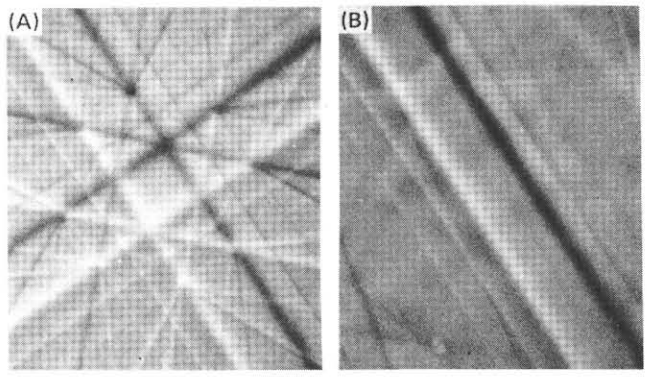

Fig. 7 Electron channeling pattern taken at the SOI layer of (A) laterally epitaxially grown region, and (B) transition region from which grain boundaries originate.