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Characterization of 0.1 μm Thick Isolated Silicon Layers on Porous Oxidized Silicon

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Physical features and electrical properties for 0.05-0.4 μm thick isolated silicon layers made by FIPOS technology were investigated. Isolated silicon layer thickness is controlled by proton implantation energy. A wedge is formed at the bottom center of the isolated silicon layer. Its thickness increment does not depend on the isolated layer thickness, but decreases as isolated silicon layer width reduces. Electrical measurement results indicate that a thin isolated silicon layer with 0.1 μm thickness has a possibility for VLSI application.

INTRODUCTION

FIPOS (Full Isolation by Porous Oxidized Silicon) provides a thin isolated silicon layer on insulator. The authors have already reported the experimental results of FIPOS/CMOS 1.3 k gate array[1] and 16 k bit SRAM[2] fabrication and showed that FIPOS is an effective technology for high performance VLSI fabrication. In these LSIs, a 0.5 μm thick isolated Si layer and 2-3 μm pattern rules were used. As the device size and pattern rule become smaller, junction depth becomes also shallower and isolated silicon thickness on the insulator must be made thinner to reduce junction capacitance.

This paper reports results of studies on the characterization of 0.05-0.4 μm thick isolated Si layers prepared by the FIPOS method. The silicon layer fabrication condition and its cross section shape are described. Next, the thickness dependencies of the field effect mobility and leakage current of MOS FETs are presented.

SAMPLE PREPARATION

Isolated Si layers were prepared by FIPOS process, as shown in Fig.1. P-type silicon wafers used were 3-5 Ω cm. The isolated Si layer thickness was controlled by proton implantation energy. Proton implantation energies used are 35-70 keV. Porous silicon of 7.0 μm thick was formed in 40 wt.% hydrofluoric acid solution. Oxidation conditions for porous silicon were 100 minutes in wet O_2 ambient at 1050 °C.

For electrical measurements, n- and p-channel MOS FETs were fabricated by n-type poly-Si gate process. After the FIPOS process, Si_3N_4 was etched off and 300 Å thick gate oxide was formed.

RESULTS AND DISCUSSIONS

Si Thickness Control The isolated silicon layer thickness depends on the n-type layer thickness formed by proton implantation and subsequently annealing. Figure 2 shows the relationship between isolated silicon layer thickness, lateral oxidation spread from the Si_3N_4 edge and proton implantation dose at 50 keV energy. As the dose increases, the thickness increases and the lateral oxidation spread decreases. Both values are constant over the $5 \times 10^{14}/cm^2$ dose.

A thousand protons are necessary to produce one donor. Since the n-type layer is not perfectly formed and the p-n junction border is out of focus in a low dose, the isolated silicon layer becomes thinner and the lateral oxidation spread becomes larger than that in a high dose. The profile for the donor produced by proton implantation has a steep slope. Therefore the isolated silicon layer thickness increment is

small,even if the implantation dose increased to more than the necessary dose to form the n-type layer. In a high dose,the lateral oxidation spread depends on the porous silicon oxidation condition,while lateral penetration of porous silicon under the Si_3N_4 film before oxidation is not observed. The lateral oxidation spread is less than 0.5 μm,which is the same as coventional selective oxidation.

The isolated silicon thickness is not uniform in FIPOS,because of the wedge structure existing in the center of the interface between the isolated layer and the porous oxidized Si. The wedge is a remained silicon positioned under the bottom center of the n-type layer when porous silicon which laterally penetrates from both side is combined. Figure 3 shows the edge and wedge thickness of the isolated silicon for 10 μm width prepared by 35-70 keV proton implantation energy. As the implantation energy increases both thicknesses increases. The increasing rates for the wedge thickness and the edge thickness are the same,i.e. the thickness difference between wedge and edge is constant,0.85 μm for 10 μm width.

On the other hand,the wedge thickness depends on the isolated silicon layer width. Figure 4 shows the relationship between the wedge thickness and the isolated silicon layer width at 60 keV. As the silicon width increases,the thickness increases. This is caused by the difference in the lateral penetration shape for various porous silicon thicknesses. The wedge width has the same tendency as its thickness. For 10 μm width isolated silicon layer, the wedge width is about 1.5 μm.

These experimental rusults indicate that the isolated silicon layer thickness can be controlled by proton energy at the implantation dose over $5x10^{14}/cm^2$ and that the thickness difference between wedge and edge does not depend on the isolated silicon layer thickness.

Electrical Characteristics of Isolated Layer

Field effect mobility was calculated from the transconductance peak value measured in the triode region in MOS FETs.

Figure 5 shows the thickness dependency of electron and hole mobility. The mobility slightly increases as thickness decreases.

In n-channel MOS FET fabrication, additional boron ion implantation for threshold voltage control was not performed. The acceptor concentration in the isolated silicon layer decreases as the thickness decreases, because of the segregation effect during the porous silicon oxidation process.

In p-channel fabrication, phosphorous ion implantation was performed before gate oxidation. Table 1 shows the phosphorous ion implantation dose for p-channel MOS FETs and measured Vth value. The Vth value increases as the thickness decreases. These results indicate that the thickness dependence of the mobility is caused by the impurity concentration.

To further crarify the relationship between Vth and mobility, mobility measurement was performed using 0.2 μm thick silicon layer.

Figure 6 shows the results. The Vth is controlled by boron or phosphorous ion implantation. As the $|Vth|$ increases,mobility decreases. Electron and hole mobility values are the same as for bulk MOS FETs. In SOS, as the silicon thickness becomes thinner, the mobility decreases because of the crystalline defect localized in the silicon-sapphire interface[3].

In FIPOS,the interface characteristics between the isolated silicon layer and the porous oxidized silicon layer do not depend on the thickness. Therefore,mobility is not changed with a change in thickness.

Next, the drain leakage current was measured for p-channel MOS FETs with W_{eff}/L_{eff} = 8.5 μm/2 μm. Measurements were performed with drain voltage at -5.0 V and gate voltage at 0 V. In each thickness, 70 FETs were measured and percentages of leakage current below 10 pA and over 1 μA were examined. As shown in Fig.7,with the decreasing thickness the percentage below 10 pA decreases and over 1μA,it increases especially below 0.1 μm thickness. The reason for the thickness dependence of the leakage current is now under investigation.

These results of leakage current yield indicate that the crystalline quality of the isolated silicon layer is excellent,even for 0.1 μm

thickness. It will be possible to apply such thinner isolated silicon layers to VLSI fabrication by making FIPOS process condition more suitable.

CONCLUSION

The cross section shape and electrical characteristics for the thin (0.05 - 0.4 μm) isolated silicon layers prepared by FIPOS have been studied.

The thickness can be easily controlled by proton implantation energy,but the ratio of the wedge thickness to the isolated layer thickness increases as the thickness decreases.

The 0.05-0.4 μm thick isolated layer mobility is the same as that for bulk MOS FETs,although leakage current yield below 10 pA decreases as the thickness decreases below 0.1 μm.

ACKNOWLEDGEMENT

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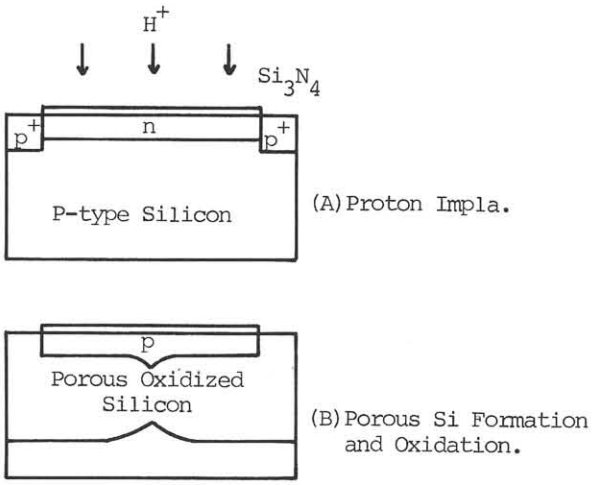

Fig.1 FIPOS process

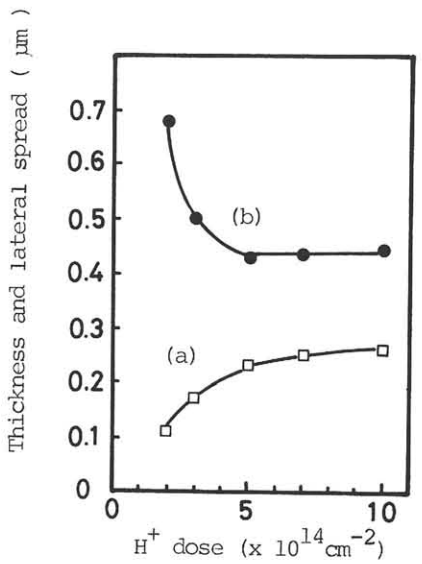

Fig.2 Proton dose dependency of Si thickness (a) and lateral oxidation spread (b).

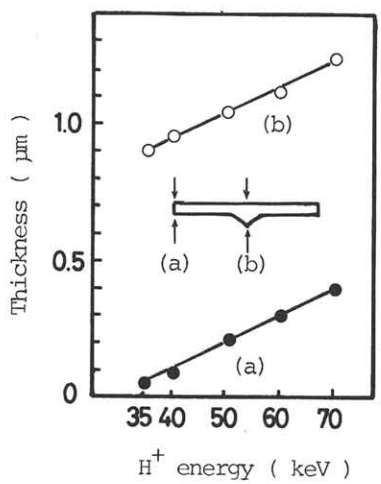

Fig.3 Isolated Si layer thickness versus proton implantation energy.

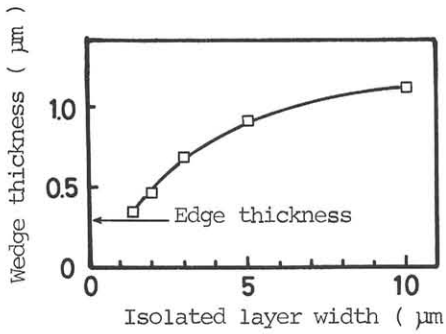

Fig.4 Isolated Si layer width dependency of wedge thickness

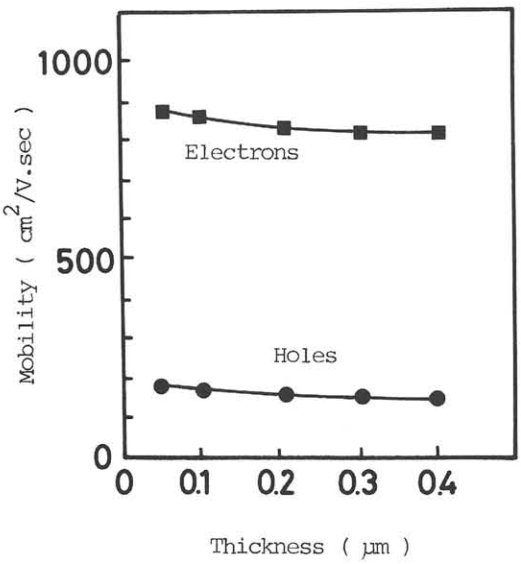

Fig.5 Mobility in 0.05-0.4 μm thick Isolated Si layer.

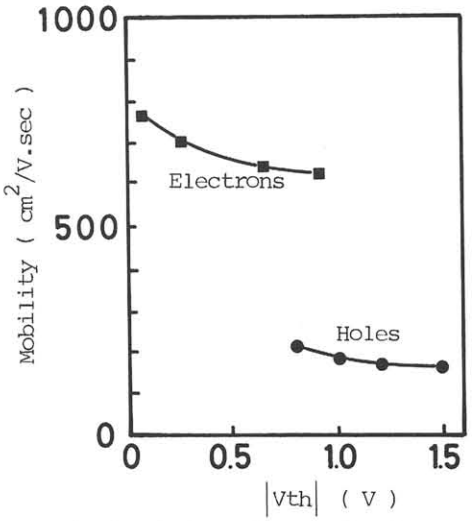

Fig.6 Vth dependency of 0.2 μm thick layer mobility.

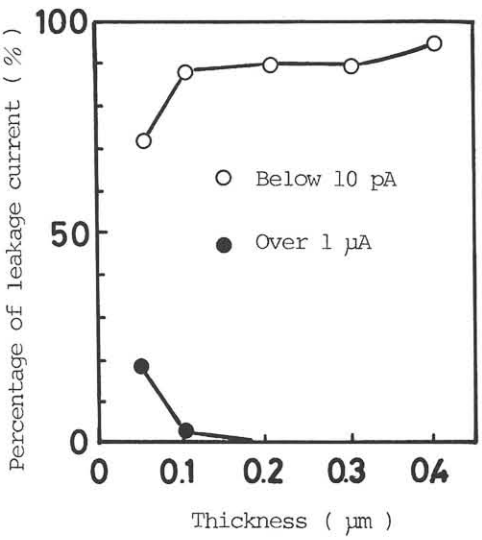

Fig.7 Percentage of leakage current for p-channel MOS FETs with W_{eff}/L_{eff}= 8.5 μm/2.0 μm.

Table 1 P-channel MOS FET fabrication condition and measured Vth value. P^+ implantation energy is 100 keV.

Thickness (μm)	P^+ dose (cm^{-2})	-Vth (V)
0.05	$3x10^{10}$	1.19
0.1	$5x10^{10}$	1.19
0.2	$2x10^{11}$	1.25
0.3	$3x10^{11}$	1.31
0.4	$5x10^{11}$	1.41