RCJL Decoder for Josephson Memory

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An RCJL (Resistor Coupled Josephson Logic) decoder was proposed and experimentally tested to satisfy the requirements for a fast and densely packaged Josephson memory. The RCJL decoder is an AC powered latch decoder and is constructed from RCJL AND-OR units. Therefore, it has advantages in regard to higher packing density, reduced decoding time and intrinsically damped resonance phenomena over interferometer decoders. A 4-bit decoder, consisting of 28 AND-OR units, was fabricated using a 4 μ m Pb-alloy technology. A ±11% bias current margin was obtained. Decoding time per stage is measured at 33 ps, when the gate bias is applied at 90 % of its maximum gate current. The dissipated power per AND-OR unit is 30 μ W.

§1. Introdcution

Josephson devices are foreseen as basic elements in an ultra high speed computer system, because of their high switching speed, low power dissipation and effectively lossless signal transmission. These features have been demonstrated by various kinds of logic circuits, such as a magnetically coupled interferometer circuit, a current injection interferometer circuit and a resistor coupled logic circuit. In these circuits, resistor coupled logic circuits have advantages in regard to circuit density, switching speed and resonance phenomena over interferometer circuits.

High speed cache memories and high density main memories have also been proposed. However, the reported access time for these memories is not fast enough to satisfy the requirement from the high speed Josephson computer system. One reason is that decoders used in these memories do not work at high speed with a wide operation margin. Address decoding in Josephson memories has been carried out with a tree decoder¹⁾, with a flip-flop decoder²⁾ or with a loop decoder 3). These decoder circuits consist of magnetically coupled interferometers and work on DC power sorce. These DC powered decoders need a reset timing signal and have a latch up problem. The latch up occurs when a reset signal overlaps the next address data signals. A time margin is necessary to prevent latch up. This results in a long decoding time. Futhermore, inductive elements in interferometors cause resonance phenomena and magnetic flux trapping.

This paper reports design and experimental evaluation for the RCJL⁴⁾ decoder, which was designed to be applied to high speed Josephson cache memories. The RCJL decoder is an AC powered latch decoder used with buffer drivers having symmetrical control characteristics. It was constructed from AND-OR units by connecting them in a tree-like configuration. The operation principle, design, fabrication process and quasi-static and dynamic measurements are reported in the following sections.

§2. Operation Principle and Circuit Design

The RCJL circuit is able to drive resistive loads in parallel, unlike magnetically coupled interferometer logic. The unit gate constructing a decoder is designed to be able to have 2 input and output signals to retain input and output current consistency which means that the sum of input currents equals the sum of output currents. Therefore, a multi stage decoder is easily designed without using buffer current amplifiers.

Figure 1 shows a blockdiagram and the circuit configuration for the AND-OR unit gate in the RCJL decoder. The AND-OR unit gate consists of a 2-input AND gate, an input-output isolation OR gate with the current amplification function, and a coupling resistor. Resistor R_A and R_B are load resistors to a preceding circuit and are designed to have 10 Ω to match transmission line characteristic impedance. Resistors $R_1 \sim R_7$ are designed so that, $R_1=2\Omega$, $R_2=R_3=R_5=R_6=R_7=1\Omega$, $R_4=1.33\Omega$ to maximize the operation region for the AND and OR gates. Resistor R_d acts to lower resonance current, which arises from switching junction J₃ and is designed at 2Ω from circuit simulation. Critical current values in junction J₁~J₆ are designed as I_{C1}=I_{C2}=0.1mA, I_{C3}=I_{C4}=0.2 mA, I_{C5}=I_{C6}=0.3 mA=I₀, respectively.

Figure 2 shows threshold characteristics for the AND gate and the OR gate used in the AND-OR unit. When a set of inputs, I_A and I_B, which correspond to a point in the shaded area in Fig. 2 (a), is applied to the AND gate, it switches. The output current, nearly equal to I_A + I_B, flows out of the AND gate into the OR gate. As shown in the Fig. 2, I_A + I_B is greater than 2/3 I₀. OR gate bias current I_b is between 2/3 I₀ and 2I₀. With input current I_A + I_B, greater than 2/3 I₀, the OR gate is fired and an output current, nearly equal to I_b, is obtained at the OR gate output terminal. To realize the input-output current consistency, the current level for I_A and I_B, and the bias current level for I_b are chosen as follows.

 $I_A \simeq I_B \simeq I_0/2$, $I_b \simeq I_0$.

A 4-bit decoder is constructed by connecting 28 AND-OR units in tree-like format, as shown in Fig. 3. Adrress signals A, B, C and D, and complimentary signals \overline{A} , \overline{B} , \overline{C} and \overline{D} , are decoded and one of the 16 outputs is selected. Because the decoder operates in a latch mode, latch up does not occur and the decoder does not need any timing signal, as is required in the loop decoder.





Fig. 1. AND-OR unit used in RCJL decoder. (a) Blockdiagram. (b) Circuit configuration.



Fig. 2. (a) Threshold characteristics for a AND gate in a AND-OR unit. (b) Threshold characteristics for a OR gate in the AND-OR unit.



Fig. 3. 4-bit decoder blockdiagram constructed by 28 AND-OR units.

§3. Circuit Analysis

Decoding delays are estimated for serially connected AND-OR units with an input signal buffer OR gate. The experimental circuit with 2 fanouts is shown in Fig. 4. The load resistance to be matched with the stripline characteristic impedance of a 4 μ m linewidth is 10 Ω . Gap voltage V_g is 2.4 mV and the product of junction subgap resistance R_{sub} and Josephson critical current is 20 mV. The capacitance for the 4 μ m diameter smallest junction is 0.4 pF. It is estimated from the measured value for a 5 μ m diameter junction. The decoding delay corresponds to a signal propagation time in an AND-OR unit and simulation is carried out across a signal buffer OR gate and a cascade chain of 3 AND-OR units. As shown in Fig. 5,



Fig. 4. Schematic diagram of 7 serially connected AND-OR units for delay measurement.



Fig. 5. Simulated and mesured decoding delays (t_d) versus common bias current $I_b\ com$ (I_b) and common AND gate input signal current $I_s\ com*$ Closed circles and A are for $I_s\ com=0.6\ I_o.$ Open circles and B are for $I_s\ com=0.35\ I_{o*}$

simulated decoding delays vary both with common bias curent $I_{\rm b}{\rm com}$ and with common AND gate input signal current $I_{\rm s}{\rm com}.$

The output current from the AND-OR unit depends on the bias current, as shown in Fig. 6. It shows the relationship $I_{out}/I_{b}=0.8$. This means that input signal isolation is accomplished by isolation junction J4 and the OR gate in the AND-OR unit is not saturated, up to a 95 % biasing.

§4. Fabrication process

The experimental RCJL decoder was fabricated using a Pb-alloy technology⁵) and a new sandwich liftoff technique (SLOT)⁶). The minimum feature size and junction diameter were 4 μ m. The AND-OR unit has a symmetrical feature for easy layout and occupies a 0.015 mm² area. The first metal layer is a 270 nm thick Nb ground plane deposited by sputtering on a



Fig. 6. Output current I $_{\rm out}$ versus normalized bias current $I_{\rm b}/2I_{\rm 0}.$

silicon substrate. The first insulating layer consists of 35 nm thick Nb₂O₅ and 150 nm thick SiO. Ground contact layer and base electrode, which are 200 nm thick lead-indium-gold alloy films, are covered by the second 270 nm thick SiO layer. The junctions are defined using the SLOT, which translates junction patterns more accurately from a mask than conventional liftoff technology. After forming the tunneling barrier by rf plasma oxidation, a 400 nm thick lead-gold counter electrode is deposited. Finally, the wiring layer, a 600 nm thick lead alloy film, is deposited without an insulating layer. AuIn2 resistor is deposited under the base electrode. The Josephson junctions with 1500 A/cm² critical current density and resistors with $0.75\Omega/\Box$ sheet resistance are used.

§5. Experimental Results

A microphotograph of the experimental 4-bit RCJL decoder is shown in Fig. 7. It has 8 address signal inputs, which are driven from off-chip drivers. An address is decoded while applying 4 address signals to 4



Fig. 7. 4-bit RCJL decoder photomicrograph.



Fig. 8. 4-bit decoding quasistatic operation.

selected address lines out of 8 address lines. Figure 8 shows decoding operation, in which address 1 is selected, when address signals A=B=C=D=1 are applied. The ± 11 % bias current margin was obtained for every address pattern. The address signal current operation region is from 0.20 mA with deviation $\sigma = 0.02$ mA to 0.49 mA with $\sigma = 0.08$ mA.

To evaluate decoding time, switching delay was measured through the chain of 7 AND-OR units connected in series, as shown in Fig. 4. Measurements were carried out in the same way⁷⁾ as that reported by Gheewala⁸⁾. When reference gate OR3 bias Ib ref=0, an input signal propagates from pulse shaper OR1 through the chain S1~S7 to output OR gate OR4. On the other hand, when reference gate OR3 is activated, the input signal passes directly from OR1 through OR3 The time interval between the output to OR4. waveforms in these two cases corresponds to the switching delay for 7 AND-OR units. The switching delay was measured versus bias current Ib com with different common address current Is com values. The measured results are plotted over Fig. 5 by estimating maximum bias current 210 from other measured threshold characteristics. The difference from the simulation comes from the 2Io estimation error. The shortest measured decoding delay was 33 psec/stage with 90 % bias current for its maximum bias current 2Io. The power dissipation, that is mainly caused in

dropping resistors, was 30 µW per AND-OR unit.

§6 Summary

Basic design aspects for the resistor coupled decoder have been investigated and the RCJL decoder was experimentally estimated. The resistor coupled decoders are AC powered latch decoder, to be used with buffer drivers. Therefore, they eliminate the timing signal, latch up problem and internal resonance problem, because of intrinsicaly possessing damping resistors. The AC power for these decoders can be supplied from the same power source as for the logic circuits. As a result, the resistor coupled decoder operates quickly and reliably.

In conclusion, a resistor coupled decoder, suitable for a high speed Josephson memory, has been developed. Experimental 4 bit RCJL decoders have been fabricated using Pb-alloy technology and new SLOT with 4 μ m minimum line width. A ±11 % bias current operation margin was obtained. The shortest measured decoding time was 33 ps per stage and measured power dissipation was 30 μ w per AND-OR unit.

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