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A 35ps Ripple Carry Josephson Adder with Latch Using High Gain Direct Coupled Logic Gates

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This paper demonstrates a new configuration for a high speed ripple carry Josephson adder circuit connected with a self-gating Josephson latch. The circuit is based on the dual rail logic constructed with high gain direct coupled logic (HDCL) gates. The configuration for the short ripple carry critical path and the wide margin latch-to-adder interconnection is proposed, and the experimental adder operation with 35ps ripple carry delay was successfully performed.

1. Introduction

Superconducting integrated circuits utilizing Josephson tunnel junctions have been foreseen as future computer devices because of their high switching speed and low power dissipation.

Current-switched logic gate constructed with Josephson junctions and resistors, especially HDCL gates which we have proposed,[1] is very attractive due to its wide operating margin, high switching speed, low power dissipation and small gate size.

An adder circuit, which is one of the basic parts in the arithmetic logic unit, requires high speed operation. A circuit with dual rail logic[2] is suited for the high speed adder application because of its timing free nature. However, a conventional dual rail adder requires about two times of a number of gates and input lines, compared with those of a single rail adder, which would cause an operating margin reduction.

In this paper, a new configuration for a high speed and wide margin adder circuit employing HDCL gates is proposed. An interconnection with a latch is also studied.

2. Design

2.1 Construction of adder with latch

Fig.1 illustrates a configuration for a full adder circuit with latches. Latch circuits, which store input data, an addend A_n and an augend B_n, at the end of a machine cycle, and generate dual rail signals, A_n, $\overline{A}_n$, B_n, and $\overline{B}_n$, at the beginning of the next machine cycle, are connected in the front stage of the adder. The adder circuit which obtains the dual rail input signals from the latch circuits and the carry from the lower bit adder circuit, generates a sum output S_n, carry outputs C_n, $\overline{C}_n$.

The latch circuit is constructed with a master flip-flop (AC F/F)[3] for storing input data in a superconducting storage loop between machine cycles, and a slave flip-flop (SGA)[3] for detecting the information stored in the storage loop. The SGA generates the dual rail outputs at the beginning of the next machine cycle and holds the outputs during the same machine cycle.

The full adder circuit is constructed with four AND gates, G1~G4; G1 is for generating a carry signal C_n, G2 is for a half adder sum signal X_n, G3 is for a carry complement signal $\overline{C}_n$, and G4

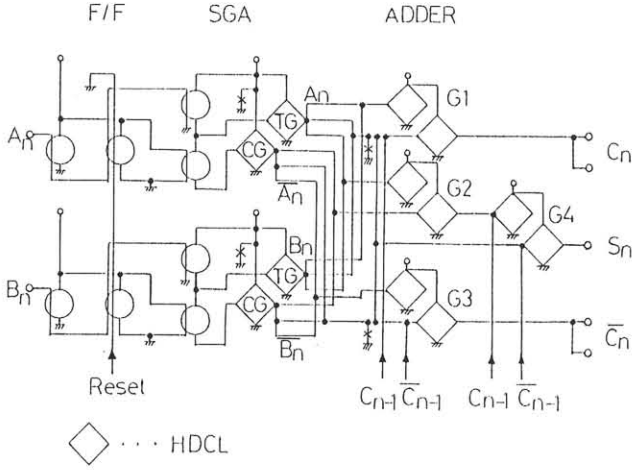

Fig.1 Configuration for a full adder circuit with latches.

is for a sum signal S_n and single Josephson junctions JJ1, JJ2 for generating $A_n \cdot B_n$ and $\overline{A}_n \cdot \overline{B}_n$ signals, respectively. The wide operating margin could be obtained by reducing the number of gates. By taking the following configuration, the number of gates could be reduced to be 60% of the conventional one.

1) The circuit is mainly constructed with "OR-AND" circuit structure instead of "AND-OR" circuit structure. In this way, the half adder sum output X_n can be obtained by only one AND gate, while "AND-OR" circuit requires two AND gates. The sum signal S_n, the carry signal C_n, and its complement $\overline{C}_n$ are generated in the similar way. 2) A simply structured AND gate that is constructed with two cascaded HDCL gates is employed. 3) The carry signals $A_n \cdot B_n$ and $\overline{A}_n \cdot \overline{B}_n$ are simply generated by the single junctions JJ1, JJ2, instead of AND gates. To realize this circuit with wide margin, buffer gates with large fan-out capability was employed in the SGA. 4) A half adder sum complementary output $\overline{X}_n$ is generated by the signals $A_n \cdot B_n$ and $\overline{A}_n \cdot \overline{B}_n$ from JJ1 and JJ2.

2.2 Shortening of critical path

For the high speed operation, the ripple carry critical path through which a carry signal from the lowest bit propagates to the highest bit should be shortened. We have constructed the ripple carry critical path with only one HDCL gate per bit by taking a circuit configuration as shown in Fig.1.

The HDCL gate delay time depends upon the parallel resistance R_T of shunt-junction J_2 in Fig.2. Computer simulation results of the switching delay time and the operating margin for the AND gate used to the ripple carry path are plotted in Fig.3 as a function of the parallel resistance R_T of the gate. Small value resistors slow down a junction switching speed which results in a larger gate delay, while large value resistors causes poor operating margin. An optimum R_T value considering the margin and delay should be chosen. At a typical design, 45ps/bit adder operation with the wide margin of up to ±30% is expected.

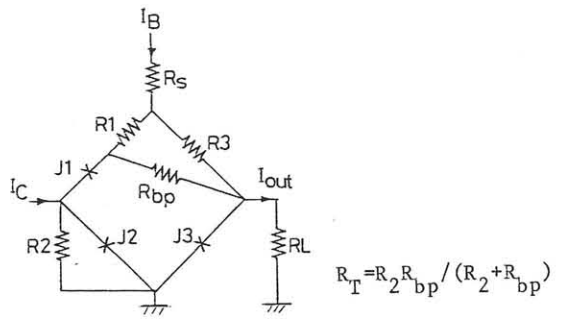

Fig.2 A high gain direct coupled logic gate.

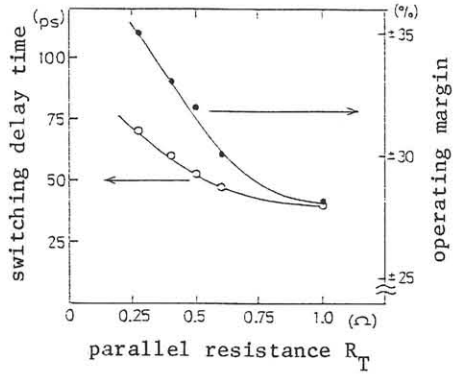

Fig.3 HDCL gate switching delay and operating margin variation with parallel resistors.

2.3 Latch-to-adder interconnection

For obtaining the wide margin latch-to-adder interconnection, the noise reduction and amplification of the signal to the adder circuit is required. It is performed by using HDCL gates for SGA output gates TG and CG as shown in Fig.1. The noise which flows into CG is caused by an incomplete isolation of the switched sense gate by which input signal to the CG should be isolated on a set condition. The noise into TG is mainly caused by the input junction switching of CG on a reset condition. To avoid the noise problem, the buffer gate should have such a threshold characteristics that switches by a input signal with a settled amplitude over a wide bias range but dose not switch by a small input signal. This characteristics is easily realized using HDCL gate which has large shunt-junction critical current I_{J2}.

The threshold characteristics of the complement output gate CG at a typical design is shown in Fig.4. To obtain the larger outputs, current levels of the buffer gates are chosen 1.5 times as large a value than that of gates used in the adder. The output signal current at the low bias current could be enough to operate the adder

circuit with the wide margin of up to ±30%. With the output gates TG and CG, the latch circuit could operate over the bias current range of up to ±26% by computer simulation.

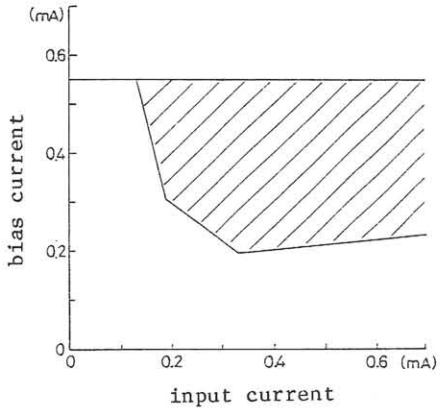

Fig.4 Threshold characteristics for CG in the SGA.

3. Experiment

In order to estimate an operating margin and carry delay time for the proposed configuration, the 2-bit parallel adder with latch and the 16-bit ripple carry adder model were fabricated by using a standard Pb alloy process of 5μm minimum line width.

3.1 2-bit parallel adder with latch

Fig.5 shows a photograph of an experimentally fabricated 2-bit adder with latch. A 2-bit parallel adder operation are successfully obtained by the experiment as shown in Fig.6. As shown in the figure, output signals for each input signals are obtained on the next cycle. this demonstrates that the latch circuit store input data on a machine cycle and adder operation is carried out successfully on the next cycle. The operating margin of the latch-to-adder interconnection was estimated by measuring the operating margin for the AND gate in the adder circuit as a function of the SGA output level as shown in Fig.7. The SGA output gates supply the current enough to drive the AND gate in the adder with the wide margin of ±27%. However, the bias margin for the latch circuit was ±7%. This narrow margin is mainly caused by the reduced loop current in the AC F/F, due to improper damping condition.

The latch could operate with a wide margin when the loop current was increased, by feeding an additional signals into the loop. From this experiment, the noise protective property of

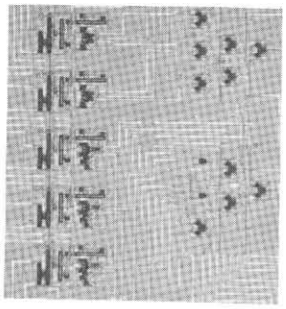

Fig.5 2-bit Josephson adder with latch.

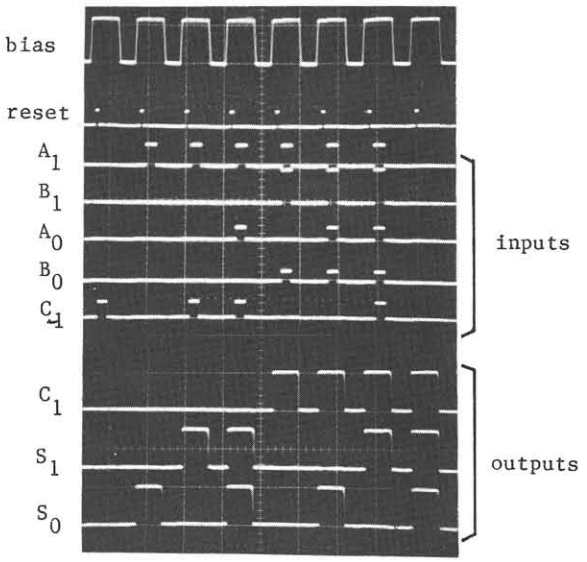

Fig.6 Operation waveforms of the adder with latch.

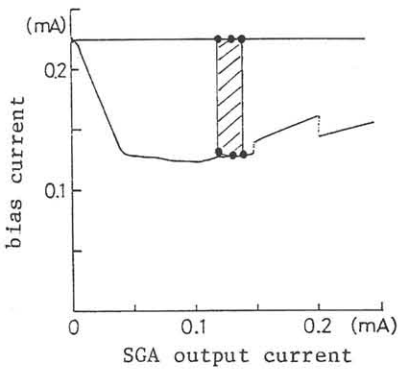

Fig.7 Measured operating margin for the interconnected AND gate.

buffer gates was verified.

3.2 16-bit ripple carry model circuit

In order to experimentally estimate the adder operating speed, the 16-bit ripple carry model which performs a following add operation; 1111...11+0000...01, was also fabricated. Fig.8 shows a microphotograph of an experimentally fabricated 16-bit ripple carry model circuit. This

circuit is constructed with two AND gates per bit; one generates a carry signal, the other is a dummy gate for the sum generator.

Fig.9 illustrates typical carry output waveforms of the first stage and ninth stage. 35 ps/bit carry delay time was experimentally obtained at the typical operating point. The experimental obtained carry delay time per bit is shown in Fig.10 as a function of the bias current. The carry delay time computed by using experimentally obtained gate parameters is represented by hatching area. In the high bias current range, the measured value agrees fairly well with the computed value. However, in the low bias range, the measured value is larger than the computed one. The reason of the difference is that the small process variation would cause larger switching speed variation at the lower bias range near the threshold.

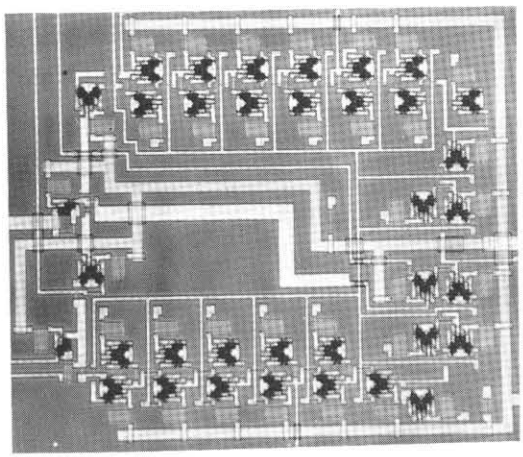

Fig.8 A microphotograph of the fabricated 16-bit ripple carry model circuit.

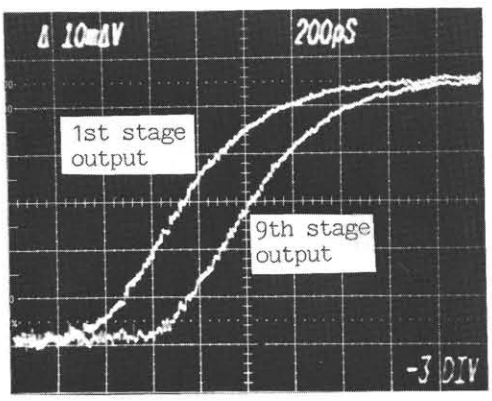

Fig.9 Measured signal waveforms of the ripple carry adder model.

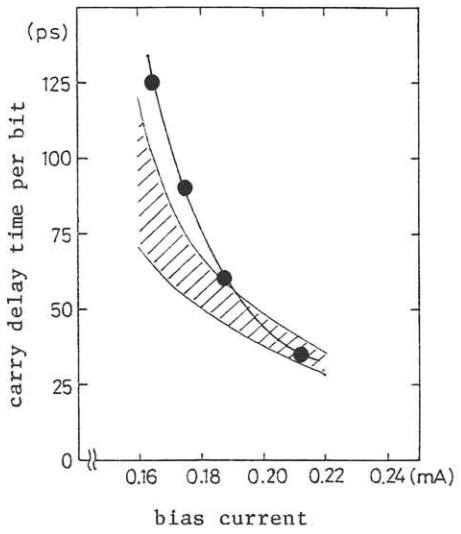

Fig.10 Ripple carry signal delay bias dependency.

The adder circuit was verified to have a small switching delay. However, switching delay of the adder was relatively large at a low bias range. Reduction in the bias level dependency of switching delay is an important problem at the next stage.

5. Conclusion

We have proposed a new configuration for a high speed Josephson adder with latch employing high gain DCL gates. The 2-bit parallel adder with latch fabricated by using a standard Pb alloy process operated satisfactorily. The experimental operating margin of the latch-to-adder interconnection as wide as ±27% was obtained. The add operating speed of 35 ps/bit was measured by 16-bit ripple carry model circuit.

6. Acknowledgment

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