Extended Abstracts of the 15th Conference on Solid State Devices and Materials, Tokyo, 1983, pp. 137-140

A-4-7

Josephson Cell Array Circuit Using Four Junction Logic (4 JL) Gates

Hiroshi NAKAGAWA, Hideo OHIGASHI, Itaru KUROSAWA, Eiichi SOGAWA,
Susumu TAKADA, and Hisao HAYAKAWA

Electrotechnical Laboratory
1-1-4 Umezono, Sakuramura, Niiharigun, Ibaraki 305, Japan

A Josephson cell array circuit composed of OR-AND unit cells based on direct coupled type Four Junction Logic gates (4JL) is described. The OR-AND cell consisting of two 2-input OR gates and a 2-input AND gate can implement fundamental logic functions with input-output current isolation capability. An 8 bit ripple carry adder with 56 cells in a 10 X 10 cell array has been fabricated with a 5 μm lead alloy technology and successfully operated with a carry propagation delay of 400 ps and a power dissipation of as low as 213 μW.

§1 Introduction

We have developed a direct-coupled type Josephson Four Junction Logic (4JL) gate in which four junctions are closely coupled in a loop without inductances.[1] The 4JL gate potentially has attractive features for logic circuits, namely, a fast switching speed, a low power dissipation, a wide margin and a small size. A logic delay of 7 ps/gate at a power dissipation of 4 μW has already been demonstrated in a 4JL gate with 2.5 μm junctions.[2] Moreover, a logic family in which an OR, an AND and an INVERTER gates are included has been developed based on the 4JL concept.[3]

In this paper, we propose an array circuit composed of OR-AND unit cells based on 4JL gates. The OR-AND cell can implement fundamental logic functions by employing dual-rail logic, and has input-output current isolation capability by itself. These properties are quite useful for realizing large scale integration circuits. An 8 bit ripple carry adder circuit has been integrated in a cell array arrangement and successfully operated at a carry propagation delay of 400 ps and a power dissipation of 213 μW.

§2 An OR-AND Unit Cell

The OR-AND unit cell is constructed with two 2-input OR gates and a 2-input AND gate.

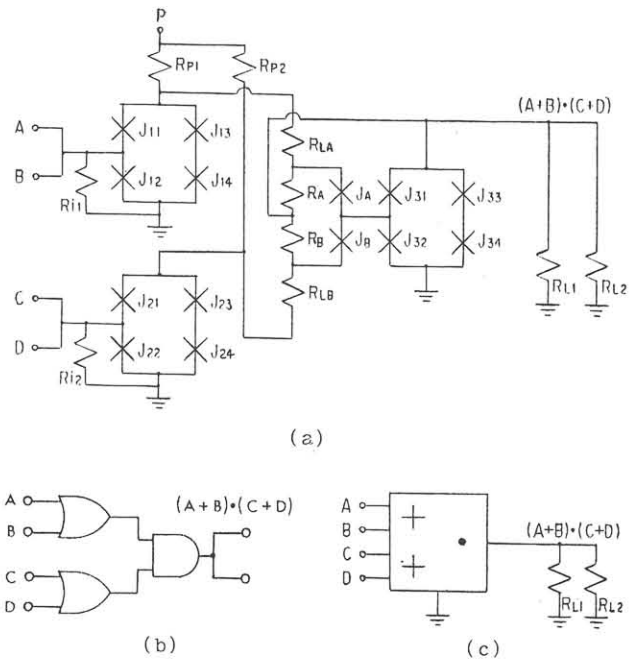

Fig.1. (a) Circuit diagram of the OR-AND cell, (b) it's logic diagram and (c) symbolic notation.

Figure 1 shows a circuit diagram of the cell with a logic diagram and a symbolic notation. This cell has a logic function $f_{cell}=(A+B)\cdot(C+D)$ for four input signals (A,B,C,D). By employing the dual rail logic, three fundamental logic operations such as OR, AND and XOR can be implemented by the cell in combination with true and complement input signals, meaning that in

Table 1. Design parameters for the OR-AND cell.

Maximum bias current	I_m	(mA)	0.56
Nominal bias current	I_p	(mA)	0.40
Operating margin	M	(%)	± 35
Power dissipation	P_{cell}	(μW)	4
Logic delay	T_d	(ps)	44

principle any logic circuits can be realized in an array arrangement of the cells.

Another important advantage of the cell is that the current isolation can be easily performed with two OR gates in front of the AND gate.

The cell has been designed to have an operating margin of ± 35% and a fanout of 2. Computer simulations show that the cell can be operated at a logic delay of 44 ps (assuming a 5 μm lead alloy junction technology) with a power dissipation of 4 μW/cell for a nominal operating condition. Design parameters of the cell is listed in Table 1.

§3. Design of An 8 Bit Ripple Carry Adder

Since the above OR-AND unit cell can implement three fundamental logic functions (OR, AND, XOR) in itself, large scale logic circuits can be easily designed by arranging the cells in an array. In order to evaluate the array circuit based on the OR-AND cell, an 8 bit ripple carry adder (RCA) circuit has been designed. In the RCA, carry (C_n,$\bar{C}_n$) and sum (S_n) generations at the n th bit are performed by following logic operations;

$$C_n=(A_n+B_n)\cdot(A_n\cdot B_n+C_{n-1}),\quad \bar{C}_n=(\bar{A}_n+\bar{B}_n)\cdot(\bar{A}_n\cdot\bar{B}_n+\bar{C}_{n-1}),$$

$$S_n=((A_n+B_n)\cdot(\bar{A}_n+\bar{B}_n)+C_{n-1})\cdot((A_n+\bar{B}_n)\cdot(\bar{A}_n+B_n)+\bar{C}_{n-1}),$$

where A_n, B_n and $\bar{A}_n$, $\bar{B}_n$ are input signals and their complements, respectively, at the n th bit. The 1 bit full adder represented by the above logic operations used in the RCA can be realized by seven unit cells as shown in Fig.2. Figure 3 shows a circuit configuration for an 8 bit RCA. In this configuration, the add time for an N bit RCA corresponds to $T_{cell}\cdot N$, where T_{cell} is a logic delay in one unit cell. Computer simulations show that the logic delay in the cell fabricated with a 5 μm lead alloy technology is 44 ps at the nominal bias condition.

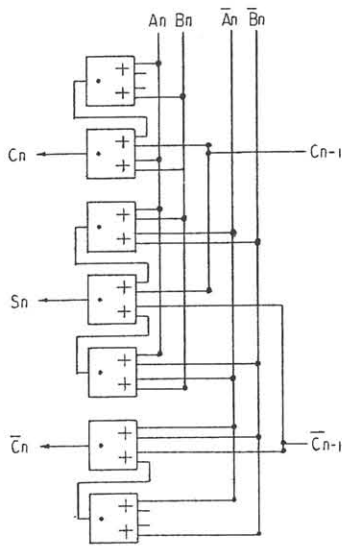

Fig.2. Circuit diagram of a 1 bit full adder used in the RCA.

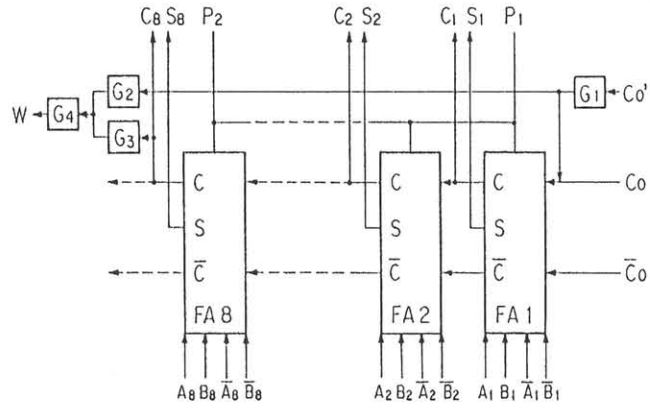

Fig.3. Circuit configuration of the 8 bit RCA. Additional four 4JL gates (G_1 G_4) are used for measurements of carry propagation delay.

§4 Operations of An 8 Bit RCA

Devices were fabricated with a 5 μm lead alloy technology. The Josephson critical current density was chosen to be 280 A/cm^2. Figure 4 shows a microphotograph of an OR-AND unit cell. The size of the cell was 165 X 175 μm^2. The maximum bias current of the unit cell was 590

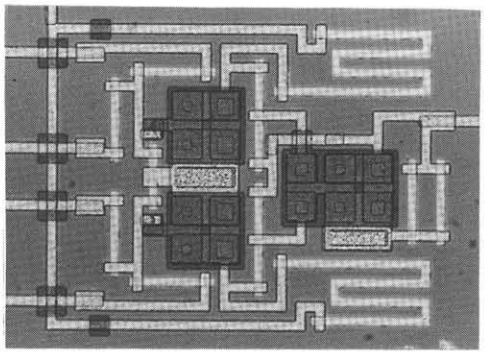

Fig.4. Microphotograph of the OR-AND unit cell fabricated using a 5 μm lead alloy technology.

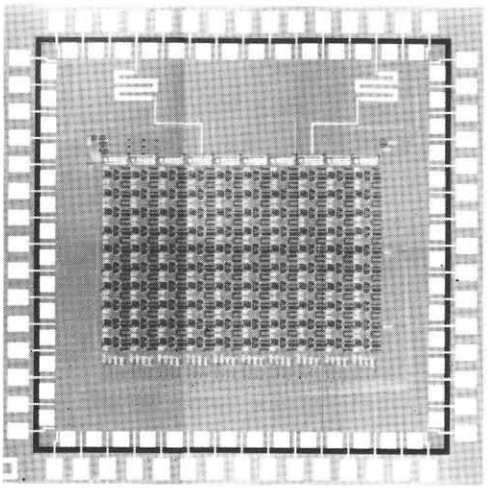

Fig.5. Photograph of a 10 X 10 cell array circuit fabricated on a 5 X 5 mm^2 Si chip. An 8 bit RCA circuit are wired using 56 cells in the array.

μA for the designed value of 560 μA. The operating margin was obtained to be ± 35% which was in good agreement with the designed one.

An 8 bit RCA was constructed by wiring 56 cells (168 gates) in a 10 X 10 cell array integrated on a 5 X 5 mm^2 Si chip. Figure 5 shows a photograph of the cell array. The 8 bit RCA was fed by two power lines, i.e., each line drove 28 cells.

Figure 6 shows results of full logic operations for the first 2 bit RCA when C_0 and $\bar{C}_0$ are set to be "0" and "1", respectively. It can be seen from Fig.6 that full adder operations are reasonably achieved in the circuit.

Figure 7 shows an example of 8 bit RCA

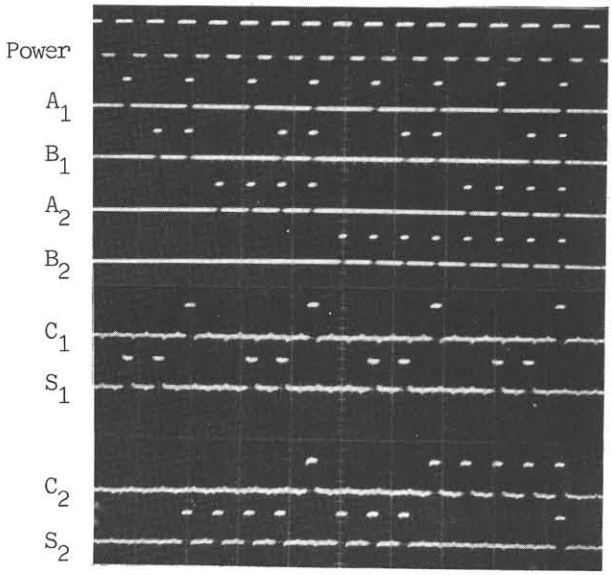

Fig.6. Full operations for the first 2 bits in the RCA obtained at a low repetition rate.

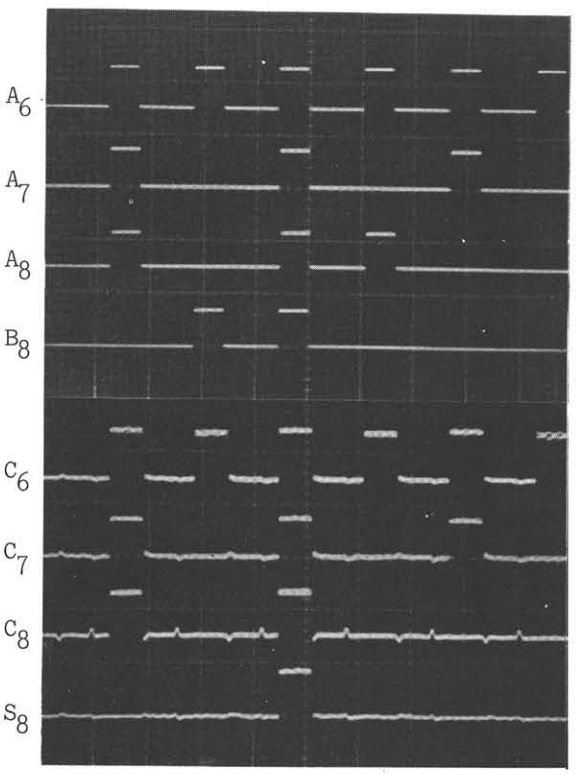

Fig.7. Examples of operations for the 8 bit RCA when ten input signals ($A_1 \sim A_8$, B_8 and C_0) were applied. In this photograph four input signal (A_6, A_7, A_8 and B_8) and output signals (C_6, C_7, C_8 and S_8) are shown.

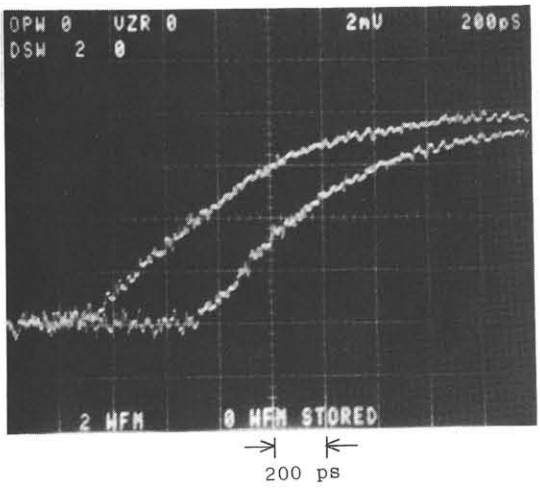

Fig.8. An experimental result of the delay measurement for the 8 bit RCA. The faster and the slower traces correspond to a bypassing signal and a propagated signal through the 8 bit RCA, respectively.

operations in the absence of complement input signals. In this example, the carry propagation was performed by applying input signals $A_1 \sim A_8$ and the sum at the 8th bit was generated by the application of an additional input signal B_8. From these experiments, it has been confirmed that the carry propagation through 8 bits are successfully carried out and the sum at the 8th bit is reasonably generated in combination with the propagated carry signal and the input signal at the 8th bit.

Carry propagation delays in the 8 bit RCA were measured from the time interval between a propagated carry signal and a bypassing one by using additional four 4JL gates ($G_1 \sim G_4$ in Fig.4). Figure 8 shows oscilloscope traces at the output gate G_4. From the time interval between two signals, the carry propagation delay for the 8 bit RCA is measured to be 400 ps, indicating that the propagation delay per bit is 50 ps. This carry propagation delay was obtained at the highest current level of 12 mA for each power line. From this current level, the average bias current to each unit cell is calculated to be 430 μA which is about 70% of the maximum bias current of the cell. The simulated propagation delay per bit at this bias condition is 44 ps. The discrepancy in delays between the theory and the experiment is mainly due

Table 2. Performance of the 8 bit RCA.

( ) : Design value.

Number of gates	168
Supply current	24 (25) mA
Carry propagation delay	400 (352) ps
Power dissipation	213 (224) μW

to process variations in the experimental circuit.

An operating margin in the 8 bit RCA was ± 10%, while ± 35% in the single OR-AND cell. The reduction of the operating margin in the RCA is attributed to process variations and noises in the measurement system.

The power dissipation in the 8 bit RCA was as small as 213 μW since the cell dissipated 3.8 μW at the bias level of 430 μA. In Table 2, the performance of the 8 bit RCA is summarized.

§5 Conclusions

We have proposed a Josephson cell array circuit composed of 4JL OR-AND unit cells which can be easily extended to LSI's. The OR-AND cell consists of two 2-input OR gates and a 2-input AND gate, which can implement fundamental logic functions such as OR, AND and XOR with input-output current isolation capability.

An 8 bit ripple carry adder circuits has been made in a 10 X 10 cell array with a 5 μm lead alloy technology. Operations have been successfully performed with a carry propagation delay of 400 ps and a power dissipation of as low as 213 μW. The Josephson array circuit developed here will be useful for integrating large scale circuits with high speeds and low power dissipations.

References

1) S.Takada, S.Kosaka and H.Hayakawa: Proc. of 11th Conf. Solid State Devices, Tokyo, 1979, Jpn.J.Appl.Phys.19(1980) Suppl.19-1, p.607.
2) H.Nakagawa, T.Odake, E.Sogawa, S.Takada and H.Hayakawa: Jpn.J.Appl.Phys.22(1983)L298.
3) H.Nakagawa, E.Sogawa, S.Takada and H.Hayakawa: Proc. of 14th Conf. Solid State Devices, Tokyo, 1982, Jpn.J.Appl.Phys.22(1983) Suppl.22-1, p.447.