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Tungsten Gate Electrode and Interconnect for MOS VLSIs

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The various properties of W and Mo films for use as MOS gates are compared. It is shown that W is superior to Mo for this purpose. In this comparison, special attention is given to metal/SiO_2 interface reaction, which might be the most important criterion when gate SiO_2 becomes extremely thin as would be the case in VLSIs such as d-RAMs with the integration density of 1Mb or higher. Next, techniques are developed for making self-aligned junctions, and for oxidizing Si without oxidizing W, something considered impossible up to now. This last technique enables the regrowth of SiO_2 around W gates, and makes this W gate process almost compatible with conventional Si technology.

§1. Introduction

Very large-scale integrated circuits (VLSI) shrink their minimum feature size to a micrometer or less and, at the same time, the number of elements per chip continue to increase. This has imposed severe demands on the material used to form gate electrodes and interconnects in MOS VLSIs. Polycrystalline silicon (poly Si) is widely used in MOS devices. However, its high resistivity causes degradation in circuit speed because of R-C delay times.

Refractory metals such as Mo and W have been proposed as an alternative.[1),2)] These metals enable the electrical resistivity at the poly Si level to be reduced by about two orders of magnitude. However, they cannot withstand high temperature oxidizing ambients during fabrication of integrated circuits, because their oxides are generally volatile. In addition, these metals can not block implanting ions during the formation of self-aligned junctions as with conventional poly Si-gate MOS technology where self-aligned junctions are produced by ion implantation with the poly Si gate acting as an implantation mask.

This study seeks to determine the most suitable material for gate electrodes and interconnects in MOS VLSIs ($\geq$1Mb). It also seeks to develop methods for producing self-aligned junctions with the metal gates and the technology that enable SiO_2 growth without oxidizing these metals.

§2. Experimental Procedures

The p-type silicon wafers, with (100) orientation and 10Ω·cm resistivity, were used as substrates to fabricate MOS devices with 20nm-thick gate oxide.

Tungsten and molybdenum films were deposited using a load-locked DC planar magnetron sputtering system.

Phospho-silicate glass (PSG) films were next deposited on these metal films by CVD, or anodic tungsten oxides were formed on the surfaces of W films in a dilute aqueous solution of 0.1N HNO_3. Tungsten or Molybdenum films were then etched to define gates in a parallel plate plasma reactor in SF_6 plasma.

Heat treatment for fabrication of MOS devices after deposition of these metals were carried out in an appropriate ambient e.g., O_2-free N_2, H_2 or H_2 with H_2O.

To analyze reactions between metals and SiO_2, ESCA (electron spectroscopy for chemical analysis), AES (auger electron spectroscopy) and SEM (scanning electron microscopy) were used. On the other hand, in-depth profiles of implanted As^+ ions in samples were measured with SIMS (secondary ion micro-spectroscopy) and C-V characteristics of MOS diodes.

§3. Results

1) Properties of W and Mo films

Comparison of W and Mo film properties is

shown in Table 1. These metals enable electrical resistivities at the poly-Si levels to be reduced by two orders of magnitude.

Molybdenum films tended to peel off from the SiO_2 substrates after patterning of gate electrodes and interconnects; whereas, good adhesion was obtained for W on SiO_2. This is because Mo films have a higher internal tensile stress than W. Stresses in W films can be controlled, from compressive to tensile, by adjusting deposition conditions (namely, Ar pressure during sputtering).

Interface reactions between the gate electrodes and SiO_2 can lead to degradation in device performance, or even failure. No reactions between these metals and SiO_2 was expected because the heat of formation of SiO_2 is more negative than those of W and Mo oxides. However, a partial reaction was observed for Mo/SiO_2 at 1000~1200°C, as shown in Fig. 1. In this figure, unoxidized Si is present for Mo/SiO_2. This was probably formed by the reduction of SiO_2 during the annealing. On the other hand, no reaction between W and SiO_2 was detected even at 1200°C.

Thus, it was concluded that W has more superior properties for gate electrodes and interconnects than Mo.

2) As^+ channeling phenomenon and its prevention

In poly-Si gate technology self-aligned junctions are generally produced by implantation through the gate oxide (SiO_2), with the poly Si-gate acting as an ion implantation mask. However, in the As^+ implantation process, W gates could not completely block As^+ and a small amount of As^+ was implanted into the Si substrate (Fig. 2). This phenomenon is called channeling. It was also observed in Mo gate technology.

Therefore, a channeling prevention technique was required to obtain W gate MOS VLSIs. Of the several methods attempted, two looked promising.

One is coating W anodic oxide thin film on the W gate. This film can prevent As^+ channeling if it is thicker than 40nm (Fig. 3). After As^+ implantation, the W anodic oxide could be reduced to W by heat treatment at about 1000°C in a H_2 ambient.

The other method is PSG coating, which can getter mobile charges in the PSG and prevent channeling. However, phosphorus oxide (P_2O_5)

Table 1. Comparison of various properties of W and Mo films

	W	Mo
Resistivity ($\times 10^{-8}\Omega\cdot m$)	11	9
Internal stress ($\times 10^9 N/m^2$)	-2*~ 0.5**	~ 0.9**
Reaction with SiO_2 in N_2 (C)	> 1200	1000 ~ 1200

*compressive **tensile
resistivity: after annealing in N_2 at 1000°C for 30min.
internal stress: as deposited

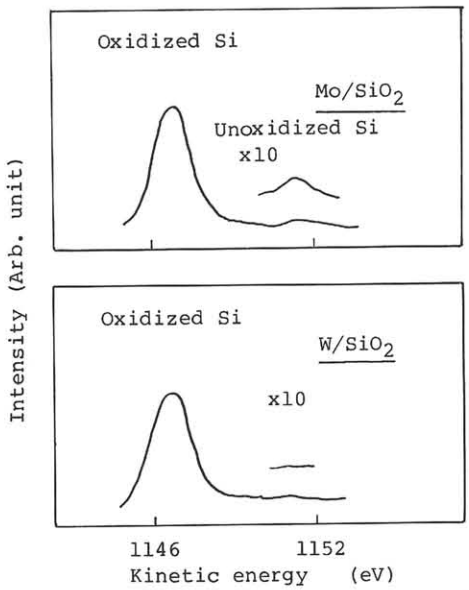

Fig. 1 Si2p ESCA spectra for surfaces of SiO_2 after removing W or Mo after annealing.
annealing: 1×10^{-5}Pa, at 1200°C for 40min

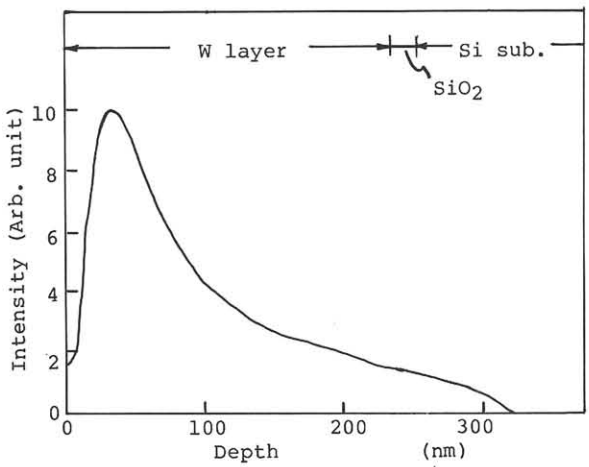

Fig. 2 SIMS depth profile of As^+ ions.
As^+ ions were implanted into W after annealing in N_2 at 1000°C for 30 min.
As^+ implantation: 80KeV, $5 \times 10^{19}/m^2$

concentration must be controlled because too high a concentration in PSG causes shifts in the flat band and threshold voltages of MOS devices (Fig. 4). This is because P diffuses through the W and gate SiO_2 into the Si substrate. The appropriate concentration of P_2O_5 in PSG is from 2 to 8 mol% if the gettering qualities and shifts of the above characteristics of MOS devices are considered.

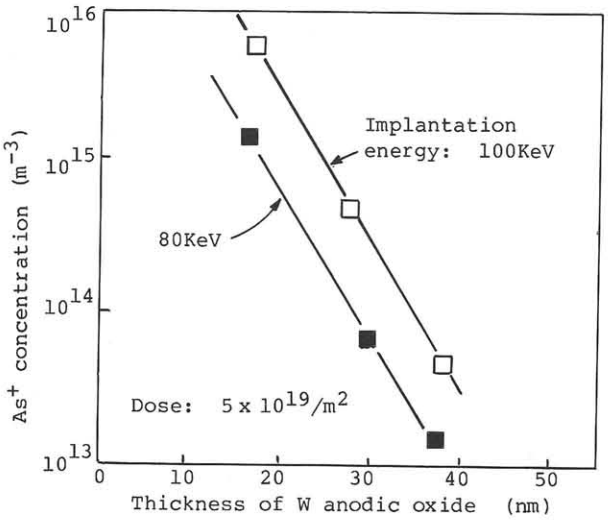

Fig. 3 Prevention of As^+ channeling by tungsten anodic oxides. Concentration at surfaces of Si substrates of As^+ ions implanted into substrates through W oxide/W/SiO_2(W/SiO_2: 226nm/20nm), obtained from C-V characteristics of MOS diodes.

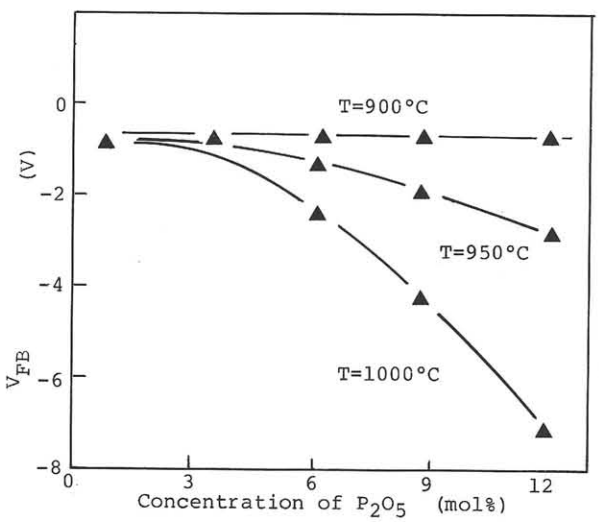

Fig. 4 Dependence of flat band voltage (V_{FB}) on P_2O_5 concentration in PSG on W. Each annealing was carried out for 30 min in N_2 at temperature T.

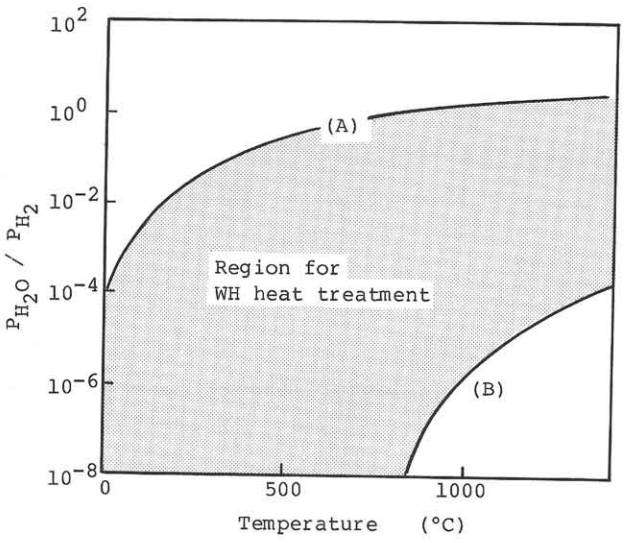

Fig. 5 Equilibrium vapor pressure ratio curves which were thermodynamically calculated for the reactions:
(A) $W + 3H_2O \rightleftarrows WO_3 + 3H_2$,
(B) $Si + 2H_2O \rightleftarrows SiO_2 + 2H_2$.
P_{H_2} : vapor pressure of H_2
P_{H_2O}: " " of H_2O

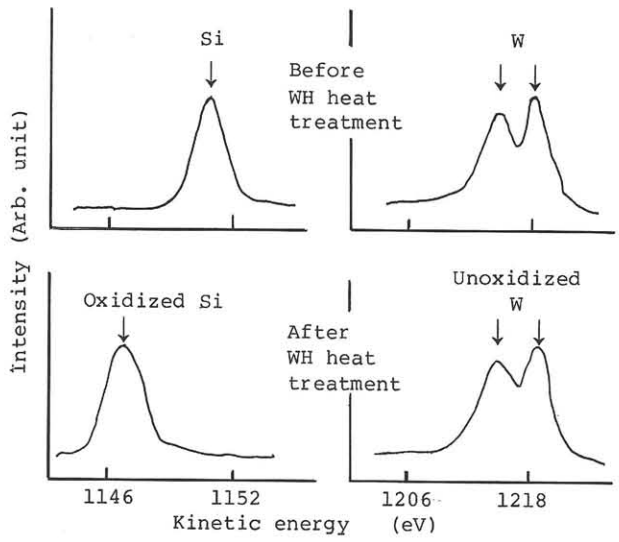

Fig. 6 Effects of WH heat treatment. W_{4f} and Si_{2p} ESCA spectra for surfaces after annealing in the ambient of H_2 with 3% H_2O at 1000°C for 40 min.

3) Regrowth of SiO_2 around W gate electrodes

The SiO_2 films around W gate electrodes may be damaged or contaminated during patterning and implantation. Thus, the dielectric integrity of the SiO_2 can become severely degraded.

In poly-Si gate technology, these SiO_2 films are usually regrown in an O_2 ambient after removal. However, similar techniques have not been

developed for refractory metal gate technologies because refractory metals have poor resistance to an oxidizing ambient.

In this work, a novel heat treatment has been developed where Si can be oxidized in the presence of W without oxidizing W. This technique is called WH (Wet Hydrogen) heat treatment. It uses H_2 atmosphere containing an appropriate amount of H_2O. The amount of H_2O added is determined from thermodynamical consideration as shown Fig. 5. Silicon can be oxidized without oxidizing W in the region between two curves of the equilibrium vapor pressure ratios, P_{H_2O}/P_{H_2}. The ESCA spectra for the surfaces of W or Si before and after WH heat treatment shown in Fig. 6 indicating the possibility of SiO_2 regrowth around W. Breakdown voltages for 20nm-thick gate SiO_2 increased by about 2V after this heat treatment as compared with that for the case without SiO_2 regrowth around W gate electrodes.

§4. Conclusions

Fabrication of highly integrated, high-performance MOS VLSIs requires new processes. Process options utilizing refractory metals as a gate instead of conventional poly Si-gate were investigated from basic considerations. Conclusions based on these results are as follows.

1) Tungsten was superior to molybdenum for use as gate electrodes and interconnects on highly integrated MOS devices, because it reacts less with SiO_2.

2) A channeling prevention technique is required to obtain W gate MOS devices. An amorphous film e.g., PSG or tungsten anodic oxide, coating on W gate can prevent the As^+ channeling phenomenon.

3) The SiO_2 regrowth around W gate electrodes without oxidizing W is possible in an atmosphere containing H_2 with an appropriate amount of H_2O.

§5. Acknowledgment

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