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Characteristics of Tungsten Gate MOSFETs for VLSIs

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This paper reports on the evaluation of MOSFETs, fabricated by tungsten gate technology. Stable and controllable threshold voltage and steep tailing are obtained, due to the good interface properties of a tungsten gate MOS structure. In addition, 0.65 V larger work function of tungsten, compared with conventional n^+-doped polysilicon, brings about some improvement in device characteristics such as a 15-20 % increase in electron mobility and 0.5 times suppressed impact ionization at the drain. These results demonstrate the feasibility of tungsten gate MOSFETs as a VLSI element.

§1. Introduction

Increased resistance of polysilicon gate electrodes and interconnect lines have constituted the circuit design constraints against realization of high performance VLSIs. Refractory metals with extremely low resistivity as well as a high melting point have become indispensable in overcoming these constraints. However, it has been very difficult to use refractory metals as a substitute for polysilicon in conventional wafer processing. This is due to undesirable properties peculiar to refractory metals, e.g., no resistance against oxidizing atomosphere, larger internal stress, and poor masking capability against ion implantation.

Development of a sophisticated wafer processing technique applicable to refractory metals[1] has already been reported. Tungsten was used, because it was most promising in terms of adhesion to SiO_2, internal stress, and reactivity with SiO_2, compared with other refractory metals.

This paper describes the device characteristics of tungsten gate MOSFETs, fabricated by this new technique. Threshold voltage, transconductance and substrate current caused by impact ionization are compared with conventional n^+-doped polysilicon gate MOSFETs. The influence of the difference in work function of tungsten and n^+-doped polysilicon on device characteristics is also discussed.

§2. Experimental

Fabricated n-channel tungsten gate MOSFETs are shown in Fig. 1. A 20 nm thick gate oxide is used here. This is indispensable in scaling down devices to the 1 μm level. Channel length was varied over a wide range, 0.5 - 30 μm. Structural dimensions are summarized in Table 1. Conventional n^+-doped polysilicon gate devices were also fabricated in the same run for the control samples.

Tungsten film deposited by planar magnetron sputtering was used in this study. Sheet resistivity of 0.3 ohm/sq. on a flat surface and less than 1.0 ohm/sq. on steep steps was obtained with 350 nm thick tungsten film.

In wafer processing, several problems peculiar to tungsten film properties occurred. Among these, the most fatal for device characteristics was implanted ion penetration through tungsten gate electrodes due to channelling. This poor masking capability against ion implantation is caused by the textured structure of tungsten film, which leads to channelling. Stacking amorphous film, such as phospho-silicate glass (PSG) or tungsten anodic oxide (WO_x), on the tungsten effectively prevented channelling.

Completed devices were evaluated by measuring threshold voltage, effective mobility, and substrate current. The two-dimensional process/device simulation using SUPREM[2] and CADDET[3]

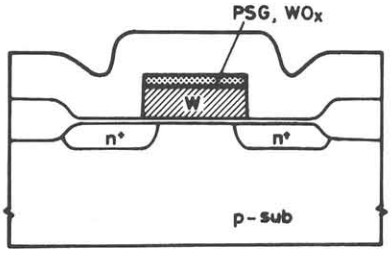

Fig. 1 Fabricated n-channel tungsten gate MOSFET structure. PSG or WO_x on tungsten is effective in preventing the penetration of implanted ions.

Table 1 Structural data of devices fabricated

Gate electrode	PSG/W, WO_x/W
Substrate	10 ohm cm (100) p-type
Gate oxide thickness	20 nm
Junction depth of S&D	0.2 um (Arsenic)
Channel length	0.5 - 30 um
Channel width	9.0 um

was also carried out to quantitatively account for the difference in tungsten gate and polysilicon gate MOSFETs device characteristics.

§3. Results and Discussions

3.1 Threshold voltage

Threshold voltage V_{th} of tungsten gate and polysilicon gate MOSFETs is shown in Fig. 2, as a function of channel implantation dose Q_{dose}. The gradient of V_{th} vs. Q_{dose} relationship of tungsten gate MOSFETs agrees closely with theoretical value q/C_{ox}, where q is elementary charge and C_{ox} is gate oxide capacitance per unit area. It can also be seen that threshold voltage of tungsten gate devices is 0.65 V higher than that of polysilicon gate MOSFETs. This V_{th} difference is consistent with the work function difference of tungsten (Φ_m = 4.75 eV) and n^+-doped polysilicon (Φ_m = 4.10 eV). In addition, the scatter in threshold voltage of tungsten gate MOSFETs was the same as that of polysilicon.

These results demonstrated the stable and controllable interface properties of our tungsten gate MOS structure. This was also affirmed by measuring tailing coefficients of tungsten gate MOSFETs. A steep tailing of 65-70 mV/decade at substrate voltage V_{BB} = -3 V was obtained, suggesting low surface states density.

On the other hand, the V_{th} lowering in the short channel region is one of the severest constraints to MOSFET miniaturization. Threshold voltage was evaluated as a function of effective channel length, as shown in Fig. 3. The channel dose of tungsten gate MOSFETs is smaller than that of polysilicon, to compensate for the work function difference. The V_{th} lowering in tungsten gate MOSFETs is just a little steeper for channel length reduction than polysilicon gate MOSFETs. This is because drain-induced surface potential barrier lowering is enhanced in tungsten gate MOSFETs due to its reduced channel dose. This is proven by 2-D process/device simulation using SUPREM and CADDET. Simulated potential distributions of a tungsten and a polysilicon gate MOSFET

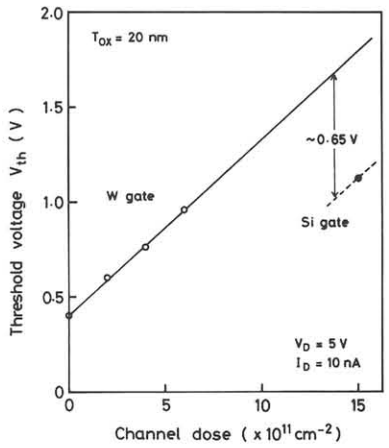

Fig. 2 Dependence on channel acceptor dose of threshold voltage V_{th} in tungsten gate MOSFETs. V_{th} of polysilicon gate MOSFETs is also shown as compared with tungsten. L_{eff} = W_{eff} = 30 μm.

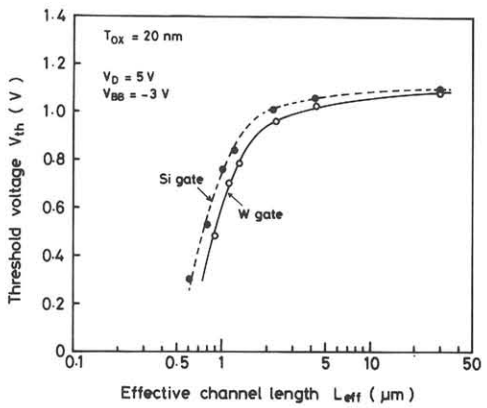

Fig. 3 Comparison between tungsten gate and polysilicon gate MOSFETs of V_{th} lowering characteristics. Threshold voltages are plotted as a function of effective channel length. V_D = 5.0 V, and V_{BB} = -3.0 V.

with a 1.0 μm effective channel length are shown in Fig. 4. It can be seen that potential in the channel region of the tungsten gate MOSFET is more affected by drain potential.

However, some degradated V_{th} lowering characteristics in tungsten gate MOSFETs could be improved using an optimized impurity profile such as buried channel structure with punchthrough stopper without any drawbacks.

3.2 Transconductance and substrate current

Improvements in carrier mobility and impact ionization characteristics are expected in tungsten gate MOSFETs, since they require a smaller channel dose than polysilicon gate devices to obtain the same V_{th}.

Typical I-V characteristics of a tungsten gate and a polysilicon gate MOSFET with a 1.0 μm effective channel length are shown in Fig. 5. Threshold voltage of each device is adjusted to 0.7 V at substrate voltage V_{BB} = -3 V. The figure shows that a tungsten gate device is superior to a polysilicon gate device in transconductance and breakdown voltage.

Transconductance of tungsten gate and polysilicon gate MOSFETs are compared as a function of effective channel length in Fig. 6. A 15-20 % increase in transconductance is demonstrated in tungsten gate MOSFETs for both linear and saturation region operation. Maximum values of effective electron mobility evaluated from Fig. 6 are

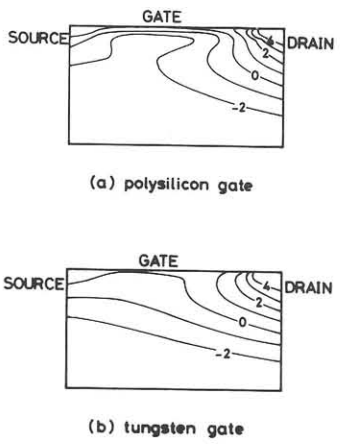

Fig. 4 Equipotential contours (normalized to 1.0 V) of (a) conventional polysilicon gate MOSFET, and (b) tungsten gate MOSFET, with L_{eff} = 1.0 μm, W_{eff} = 9.0 μm, and T_{ox} = 20 nm. Each device operates at the threshold voltage. V_D = 5.0 V, and V_{BB} = -3.0 V.

570 cm^2/V sec for tungsten gate MOSFETS and 480 cm^2/V sec for polysilicon gate MOSFETs. This improvement in transconductance can be explained by reduced impurity scattering as well as weakened electric field, due to its reduced channel dose.[4)]

Substrate current of a tungsten gate and a polysilicon gate MOSFET with a 1.0 μm effective channel length are shown in Fig. 7. A tungsten gate MOSFET has 0.5 times lower peak value of substrate current compared with a polysilicon gate MOSFET for a given drain voltages. This meas that the electric field at the drain which causes the impact ionization is certainly weakened in a

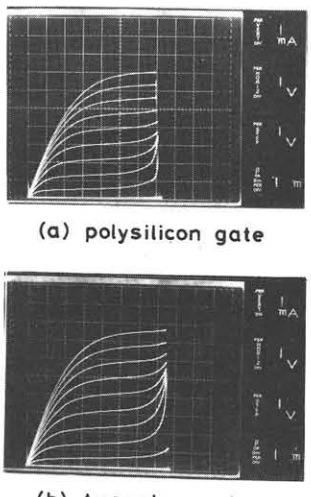

Fig. 5 I-V characteristics of (a) conventional polysilicon gate MOSFET, and (b) tungsten gate MOSFET, with L_{eff} = 1.0 μm, W_{eff} = 9.0 μm, and T_{ox} = 20 nm. V_{th} of each device is adjusted to 0.7 V, at substrate voltage V_{BB} = -3 V.

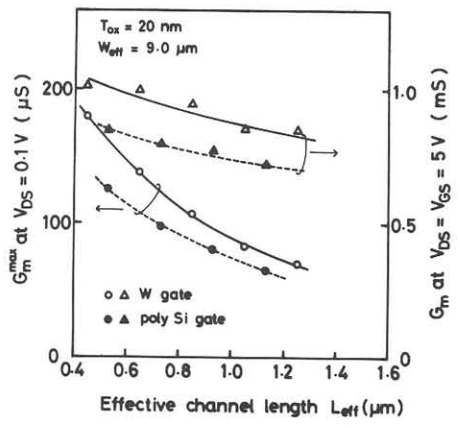

Fig. 6 Comparison of transconductance characteristics of tungsten gate and polysilicon gate MOSFETs as a function of effective channel length.