tungsten gate MOSFET, due to reduced channel acceptor concentration. Suppression of impact ionization, even by a factor of 2, is quite appreciable in improving the reliability, especially long-term degradation due to hot-carrier generation.[5),6)]

Breakdown drain sustaining voltage of tungsten gate and polysilicon gate MOSFETs are also shown in Fig. 8. Tungsten gate MOSFETs represent a 0.5 V increase in breakdown voltage. This reflects the suppressed substrate current.

§4. Conclusion

Device characteristics of MOSFETs with a tungsten gate have been described. Stable and controllable threshold voltage and steep tailing are obtained due to the good interface properties of a tungsten gate MOS structure. In addition, tungsten gate MOSFETs have improved characteristics of 15-20 % larger effective electron mobility and 0.5 times suppressed impact ionization at the drain, compared with conventional n^+-doped polysilicon gate MOSFETs. These advantages, due to larger work function of tungsten, are appreciable in device performance and reliability.

On the other hand, V_{th} lowering is somewhat enhanced in tungsten gate MOSFETs due to its reduced channel dose. However, this could be improved by using an optimum impurity profile such as buried channel structure without any drawbacks.

Thus, it has been proven that tungsten gate MOSFETs are quite feasible as a VLSI element.

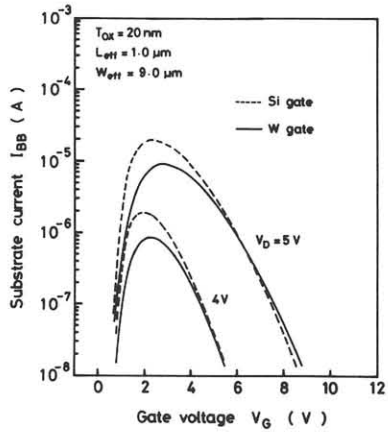

Fig.7 Comparison of substrate current of a tungsten gate and a polysilicon gate MOSFET as a function of gate voltage.

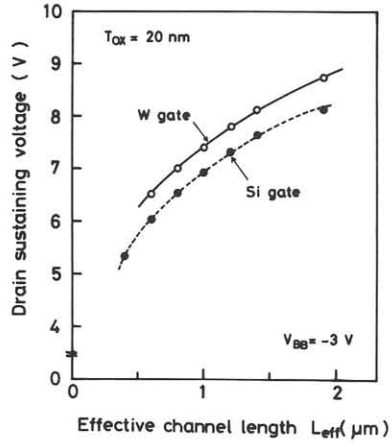

Fig. 8 Comparison of breakdown drain sustaining voltage of tungsten gate and polysilicon gate MOSFETs as a function of effective channel length.

References

1) N. Yamamoto et al., in this issue.
2) R. W. Dutton et al., IEEE J. Solid State Circuits, SC-14 (1979) 412.
3) T. Toyabe et al., IEEE Trans. Electron Devices, ED-26 (1979) 453.
4) K. Yamaguchi, IEEE Trans. Electron Devices, ED-26 (1979) 1068.
5) E. Takeda et al., IEEE Trans. Electron Devices, ED-29 (1982) 611.
6) E. Takeda et al., 1982 VLSI Symposium Digest Paper, 40.

Extended Abstracts of the 15th Conference on Solid State Devices and Materials, Tokyo, 1983, pp. 225-228

A-6-3

A New Encroachment-Free Tungsten CVD Process with Superior Selectivity

T.Moriya, K.Yamada, Y.Tsunashima, S.Nakata, and M.Kashiwagi

Toshiba Research and Development Center, Toshiba Corporation
72 Horikawa-cho, Saiwai-ku, Kawasaki 210, Japan

A selective W-CVD process applicable to Si VLSI's with a minimum feature size of 1 micron or below has been developed. Sheet resistance of shallow As-diffused layers of 0.2 micron junction depth was lowered to 1 ohm/square by self-aligned surface metallization with 1200A W film, without any junction deterioration. Problems inevitably encountered in W-CVD employing WF_6 such as encroachment at pattern edges along SiO_2/Si interface, deposition selectivity between Si and SiO_2, and deposition thickness limitation were discussed especially in relation with deposition parameters, and solutions for them were made clear.

1 Introduction

The reduction of device feature size brings about electrical resistance increase in interconnections which restricts device switching speed. Consequently, poly-silicon, widely used gate and interconnecting material, is getting replaced by refractory metal and/or their silicides. Further progress in the device feature size reduction needs very shallow source/drain diffused layers of a low sheet resistance as well as low resistance interconnections.

In W-CVD employing WF_6, it is known that W deosits selectively onto Si in a patterned Si substrate where the substrate surface is covered partially with SiO_2.[1] This selective W-CVD has a possibility to lower the resistance of source/drain diffused layers as well as poly-silicon interconnections, and some works were done on its application to silicon devices.[2),3] W-CVD employing WF_6, however, has a crucial problem for the application to small size devices. It is encroachment at pattern edges which extends along SiO_2/Si interface during W-CVD.

In this paper, we describe W-CVD process which enables W deposition onto diffused layers without any harmful encroachment as well as with a sufficient selectivity.

2 Experimental

W was deposited from WF_6-Ar or WF_6-H_2 utilizing a hot wall LPCVD reactor. A quadrapole mass spectrometer was connected at the reactor outlet to analyze the chemical species in the reacted gas. The depositions were carried out at the deposition temperature of 150-600°C, the WF_6 partial pressure of 1×10^{-4}-2×10^{-3}Torr, and the reactor total pressure of 0.1-0.2Torr. 4-inch, p-type, (100) Si wafers were employed as deposition substrates, and, in order to study the encroachment and the deposition selectivity, SiO_2 was thrmally grown and patterned with RIE. The deposited W thickness ranging in 50-5000A was measured with Taly-Surf. The encroachment was obseved with SEM and the leakage current of W deposited As-diffused diodes was evaluated to check the applicability to small size devices of shallow junction depth.

3 Experimental Results and Discussion

3-1 W deposition onto Si

The deposition time dependence of W deposition thickness is shown in Fig.1 for both reaction gases, WF_6-Ar and WF_6-H_2. In case of WF_6-Ar, at the initial deposition stage, W deposition proceeds rapidly to the thickness determined by the deposition temperature, and, after that, deposition scarcely proceeds. On the other hand, in case of WF_6-H_2, the initial deposition behavior is the same as WF_6-Ar, however, following the initial stage, deposition continues in linear dependence with deposition time.

At the initial deposition stage, SiF_x^+, fragment from SiF_4, was observed in the reacted gas for both cases. In Fig.2, mass peak height change during deposition was shown of main species in the reacted gas for both cases. From these results, the followings are deduced. At the initial stage, WF_6 is reduced by Si in the reaction,

$$WF_6 + 3/2\,Si \rightarrow W + 3/2\,SiF_4 \qquad (1)$$

and, once the substrate surface is covered with deposited W and/or Si supply from the substrate through deposited W becomes so small, deposition ceases in case of WF_6-Ar, however, in case of WF_6-H_2, deposition continues in the reaction,

$$WF_6 + 3\,H_2 \rightarrow W + 6\,HF \qquad (2)$$

Since the reaction (2) takes place at W surface, W surface is considered to have some catalyzing effect on the reaction (2), and it is the very origin of selective deposition by the reaction (2).

The deposited W thickness and the Si thickness consumed by the reaction (1) are shown in Fig. 3 as a function of the deposition time. The consumed Si thickness was estimated from the weight difference before and after the etching removal of deposited W on Si substrate. It is noted that the deposited W thickness is always smaller than the consumed Si thickness as expected from the reaction (1) if the densities of Si and W considered.

3-2 Encroachment at pattern edges

When W deposition was done onto a patterned substrate employing WF_6-Ar, encroachment was observed to take place at the pattern edges along SiO_2/Si interface as shown in Fig.4. The encroachment is enhanced with the depostion temperature elevation and/or the WF_6 partial pressure increase, and extends in proportion to the deposition time as shown in Fig.5.

Since the deposited W surface is merged into the substrate because of the reaction (1) as mentioned at the last part of 3-1, a small gap is produced between SiO_2 and Si at the pattern edges, and, subsequently, W deposits into the gap, producing a further gap. The continuation of the gap formation and the subsequent W deposition into the gap leads to the encroachment along the SiO_2/Si interface from the pattern edges. Even in case of WF_6-H_2, the encroachment occurs only at the initial deposition stage.

Though the encroachment is not able to be avoided essentially in W selective deposition, an adequate choice of deposition parameters makes it possible to suppress the encroachment to the extent where it brings about no problem in the application to small size devices. By employing WF_6-H_2 and optimizing the deposition parameters such as WF_6 partial pressure and deposition temperature, the encroachment was suppressed to below detectable level.

3-3 Deposition selectivity in WF_6-H_2

In case of WF_6-Ar, W deposition never occurs on SiO_2 because the reaction (1) is not able to proceed on SiO_2, and, therefore, the deposition selectivity is perfect. On the other hand, in case of WF_6-H_2, as W deposition proceeds onto Si, mound-like deposition comes to be observed on SiO_2, as shown in Fig.6, especially near the pattern edges. This kind of deposition on SiO_2 is never observed if there is not any Si in the reactor which is directly revealed to the reaction gas, WF_6-H_2. This means that the reaction product of the reaction (1) such as SiF_4 causes nucleation sites on SiO_2 for the deposition by the reaction (2).

To obtain a high deposition selectivity between Si and SiO_2, it is necessary to minimize the reaction (1) and scavenge the reaction product from the substrate surface as prompt as possible.

By optimizing the total pressure in the reactor for selectivity, the deposition temperature for encroachment suppression, and the WF_6 partial pressure for both, W deposition was done onto a As-diffused layers defined with LOCOS oxide mask, and W film of 800-1200A thickness was deposited without any deposition on SiO_2, namely in a perfect selectivity. In spite of so shallow junction depth of 0.2 microns, the I-V characteristics of the diodes showed no deterioration as shown in Fig.7, which indicates nearly perfect suppression of the encroachment.

4 Summary

In W-CVD employing WF_6 only, W deposition proceeds in a reduction reaction by Si and the deposition selectivity between Si and SiO_2 is perfect, however, the maximum W thickness obtained is limited by the deposition temperature and a crucial encroachment is inevitably caused at the pattern

edges along the SiO_2/Si interface, which makes it impossible to apply the CVD process to small size devices. H_2 addition to WF_6 has a tendency to deteriorate the deposition selectivity, however, it improves so much the problems of the film thickness limitation and the encroachment at pattern edges.

By making an adequate optimization of the deposition parameters in W-CVD employing WF_6-H_2, W was deposited onto a As-diffused layer to the thickness of 1200A and without any deposition on SiO_2, and thus formed diodes of 0.2 micron junction depth showed no deterioration in their I-V characteristics.

Since the deposited W has resistivity of 1.2 x 10^{-5}ohm-cm, this W-CVD process enables to lower the sheet resistance of the diffused layer to 1 ohm/square as well as poly-silicon interconnections.

These results is suggesting the applicability of this W-CVD process to Si VLSI's with a minimum feature size of 1 micron or below.

The authors wish to thank T. Shibata for the critical reading of this paper and the fruitful discussion, and M. Toyama and the colleagues of Integrated Circuts Lab. for the encouragement in the course of this work.

REFERENCES

1. J.M. Shaw, and J.A. Amick, RCA Rev., June(1970), p306.
2. P.A. Gargini, and I. Beinglass, IEDM Tech. Digest, Dec.(1981), p54.
3. N.E. Miller, and I. Beinglass, Solid State Tech., Dec.(1982), p85.

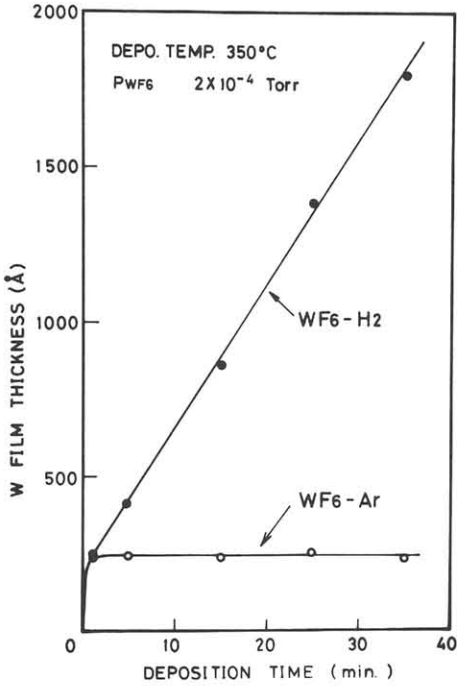

Fig.1 Deposition time dependence of deposition thickness.

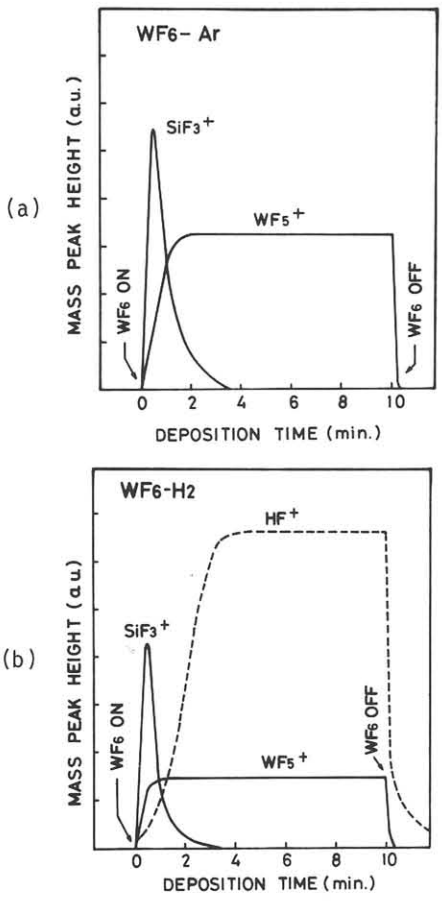

Fig.2 Changes in mass spectrometer peak height of main chemical species in reacted gases, (a) WF_6-Ar and (b) WF_6-H_2, during deposition.

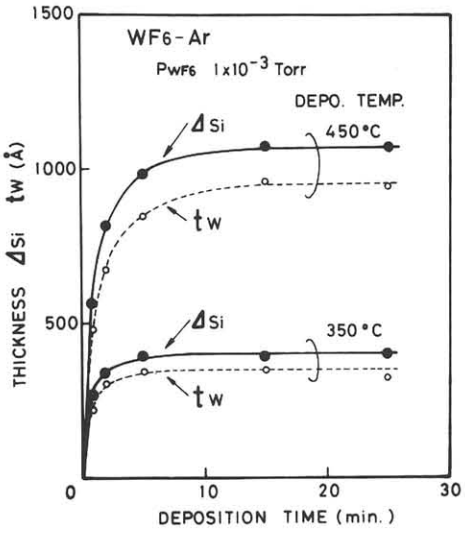

Fig.3 Deposition time dependence of deposited W thickness and consumed Si thickness.

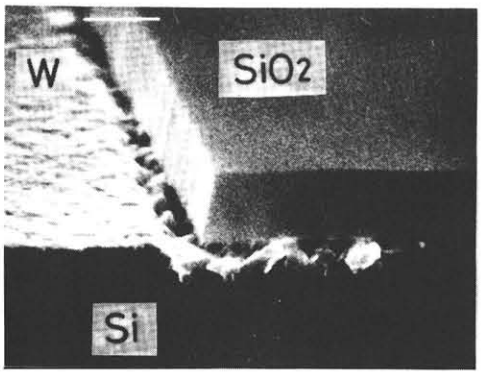

Fig.4 Cross sectional view of encroachment at pattern edge. Deposition temperature: 500°C. WF_6 partial pressure: 1 x 10-3Torr. Deposition time: 15min.

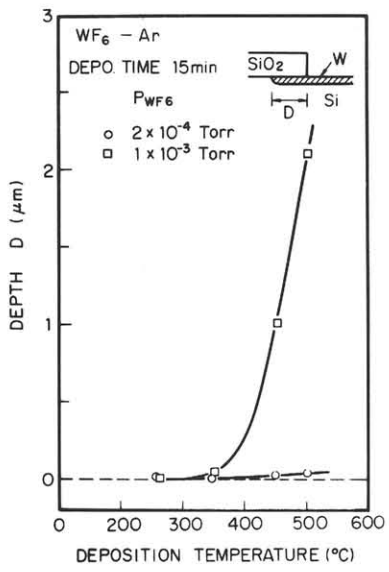

Fig.5 Deposition temperature dependence of encroachment.

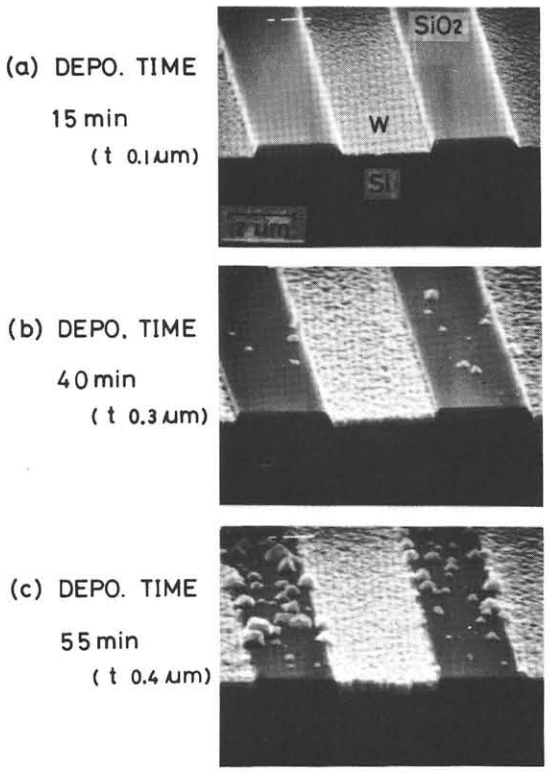

Fig.6 Deterioration of deposition selectivity with deposition progress in WF_6-H_2. Deposition temperature: 400°C. WF_6 partial pressure: 2×10^{-4}Torr.

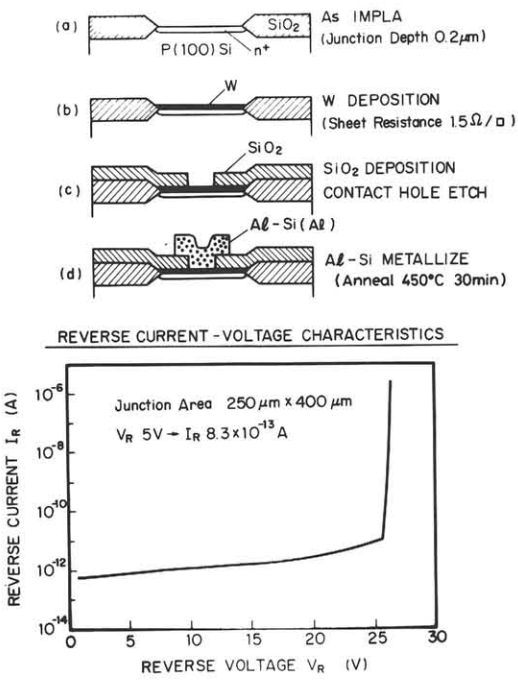

Fig.7 I-V characteristics of As-diffused n^+p diode with surface metallized by 800A W deposited film.