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Two Step Deposition Method for Reducing Surface States of Mo Gate MOS Devices with Thin Gate Oxides

T.Amazawa and H.Oikawa

Atsugi Electrical Communication Laboratory, Nippon Telegraph and Telephone Public Corporation, Atsugi-shi, 243-01 Japan

Surface State generation caused by Mo penetration into the Si-SiO_2 interface during Mo deposition has been investigated. To prevent the Mo penetration, we have proposed a new Mo deposition method which we call the "Two Step Deposition Method". In this method, Mo is very thinly deposited at a low temperature to form a conductive layer, and thick layer of Mo film is subsequently deposited at a high temperature. The Mo penetration depth in SiO_2 is reduced to less than 30 Å, and surface state density is reduced to below $3X10^{10}$ $cm^{-2}v^{-1}$ even in MOS devices with gate oxide thickness of about 100 Å.

1. Introduction

Mo gate MOS technology has been attracted special interest as one of the key technologies for VLSI development. However, Mo penetration into gate SiO_2 during Mo deposition has recently been observed, and it has been shown that the penetration of Mo atoms causes surface state generation in Mo gate MOS structures.(1) The Mo penetration phenomenon becomes a serious problem as the gate SiO_2 thickness of MOS LSI decreases. We have developed a new Mo deposition method to prevent the Mo penetration, which we call the "Two Step Deposition Method". By using this method, the Mo penetration depth in SiO_2 is reduced to less than 30 Å.

This paper describes the feature of the two step deposition method as well as the relationship between the Mo penetration phenomenon and surface state generation. Characteristics of Mo gate MOS devices with thin gate SiO_2 are also presented.

2. Surface state generation caused by Mo penetration into the Si-SiO_2 interface

Mo penetration into SiO_2 has been investigated using SIMS analysis. Measured samples are prepared as follows: Mo films are deposited on thermally grown SiO_2 by DC magnetron sputtering, electron-beam evaporation or chemical vapor deposition (CVD) methods. Then, the Mo films are removed by wet etching with a H_2SO_4 and H_2O_2 solution, and subsequently the SiO_2 surfaces are etched off to different depths with a 0.5% hydrofluoric acid solution. Detected ion counts of $^{98}Mo^+$ on the SiO_2 surfaces are plotted for etching depths of SiO_2. Figures 1(a) and (b) show the results for sputtering and evaporation. When the substrate is not heated during deposition (T_S = 25 °C), no Mo is detected on the SiO_2 surface etched off to a depth of 30 Å. However, if the substrate is heated to more than 200 °C, Mo penetration is observed. The penetration depths for sputtering are smaller than those for evaporation. When Mo film is deposited on SiO_2 by CVD method, Mo is not observed in SiO_2, although the substrate temperature during deposition is as high as 650 °C.

Next, Mo diffusion depth into SiO_2 has been estimated for annealed samples with Mo/SiO_2 structure. Figure 2 shows the result for samples in which Mo have been deeply penetrated into SiO_2 by electron-beam evaporation at substrate temperature of 400 °C. No difference in Mo profiles is observed before and after annealing at 1000 °C for 30 minutes. Furthermore, with regard to the CVD-Mo/SiO_2 structure, Mo was not detected in SiO_2 even after annealing at 1100 °C for 3 hours. From the above results, it is concluded that Mo atoms do not diffuse into SiO_2 at high temperature annealing of about 1100 °C.

Figure 3 shows gate oxide thickness d_{ox}

dependencies of surface state density N_{SS} in Mo gate MOS diodes fabricated using electron-beam evaporation. N_{SS} increases with an increase in T_S and with a decrease in d_{ox}. By comparing Figs.1(b) and 3, it is found that Mo penetration depths agree quite closely gate oxide thicknesses at which surface states are generated. Therefore, surface state is considered to be generated by Mo atoms penetrated into Si-SiO_2 interface.

3. Two step deposition method

In the fabrication of Mo gate MOS LSIs, Mo films are usually deposited by either sputtering or electron-beam evaporation. Substrate heating during the Mo deposition is essential to improve Mo film properties such as resistivity and step coverage. However, when the substrate is heated to more than 200°C during Mo deposition, Mo penetration into SiO_2 and surface state degradation occur.

The Mo penetration mechanism into SiO_2 is not clear at present. It cannot be explained by a simple diffusion mechanism, because Mo does not diffuse into SiO_2 even by annealing at 1100°C. From the facts that the Mo penetration phenomenon does not occur in the CVD method, and that Mo penetration does occur during the deposition of several Mo atom layers immediately after the start of deposition, we consider that this penetration is related to electric charges such as electrons on the SiO_2 surface. In accordance with this assumption, if a conductive layer exists on the gate SiO_2 before deposition, Mo penetration is expected to be prevented because the charges escape from the SiO_2 surface. Based on this idea, we have developed the "Two Step Deposition Method", which is shown in Fig.4. In the first deposition step, Mo is very thinly deposited at a low temperature to form a conductive layer. In the second step, a thick layer of Mo film is deposited at a high temperature to obtain good film properties.

Figure 5 shows the dependence of Mo film resistivity on film thickness. Mo film thicknesses are determined from deposition time, since the film thickness above 100 Å is confirmed to be exactly proportional to the deposition time from Talystep measurements. The solid line in Fig.5 is a theoretical curve based on the considerations of film surface scattering and grain boundary scattering of conduction electrons. P and R are the fraction of conduction electrons specularly scattered at the external surface and the reflection coefficient of electrons at the grain boundaries in the film, respectively. Above Mo film thickness of 30 Å, the theoretical curve fits the experimental points for P=0 and R=0.11. Therefore, Mo atoms are considered to contribute to the formation of uniform film even for small thicknesses of about 30 Å. It is remarkable that the Mo film is conductive, even when the film thickness is only 10 Å. In the two step deposition, surface charges on SiO_2 can easily escape through the first Mo layer having a thickness of 10 Å.

Figure 6 shows the relationship between the flat-band voltage V_{FB} of a Mo gate MOS diode and the thickness d_{Mo1} of the first layer Mo film in the two step deposition method. V_{FB} is improved at a Mo film thickness of about 10 Å and becomes a constant value at above 20 Å. This result corresponds to the experimental results of the conductivity for thin Mo film shown in Fig.5. Figure 7 shows the SIMS depth profiles of Mo in the SiO_2 for the two step deposition. The Mo penetration depth is reduced to below 30 Å.

From above results, it is concluded that Mo penetration into SiO_2 is easily prevented by the two step deposition with a very thin conductive layer.

4. Characteristics of Mo gate MOS devices with thin gate oxide

MOS characteristics of Mo gate MOS diodes with thin gate oxides fabricated using the two step deposition method have been evaluated. Figure 8 shows the surface state density distribution of a MOS diode with a gate oxide thickness d_{ox} of 100 Å. For the MOS diode fabricated by the conventional evaporation at a substrate temperature of 550°C, surface state density is near $10^{12}cm^{-2}eV^{-1}$. For the two step deposition, however, the surface state generation is not observed. Furthermore, the gate oxide thickness dependence of breakdown strength E_{BD} for the MOS diode fabricated by the two step deposition was measured. E_{BD} was about 10^7 V/cm even for the MOS diode with a d_{ox} of 60 Å.

By using the two step deposition method,

the characteristics of Mo gate MOS diodes with gate oxide thickness of about 100 Å have been improved.

5. Summary

Mo penetration into SiO_2 during Mo deposition at high substrate temperatures has been investigated in detail. A surface state is generated in a Mo gate MOS diode due to Mo penetration into the Si-SiO_2 interface. This penetration is assumed to be related to charges such as electrons. To prevent this Mo penetration into SiO_2, we have developed a new deposition method, which we call the "Two Step Deposition Method". In this method, Mo is very thinly deposited at a low temperature to form a conductive layer in which Mo does not penetrate, and after that a thicker layer of Mo film is deposited at a high temperature. MOS characteristics of Mo gate MOS devices fabricated using the two step deposition method are excellent even for gate SiO_2 thickness of 100 Å.

This two step deposition method is very effective in the fabrication of Mo gate MOS LSIs with very thin gate SiO_2.

Acknowledgements

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Reference

(1) H.Oikawa et al : Tech. Digest of IEDM,564(1982)

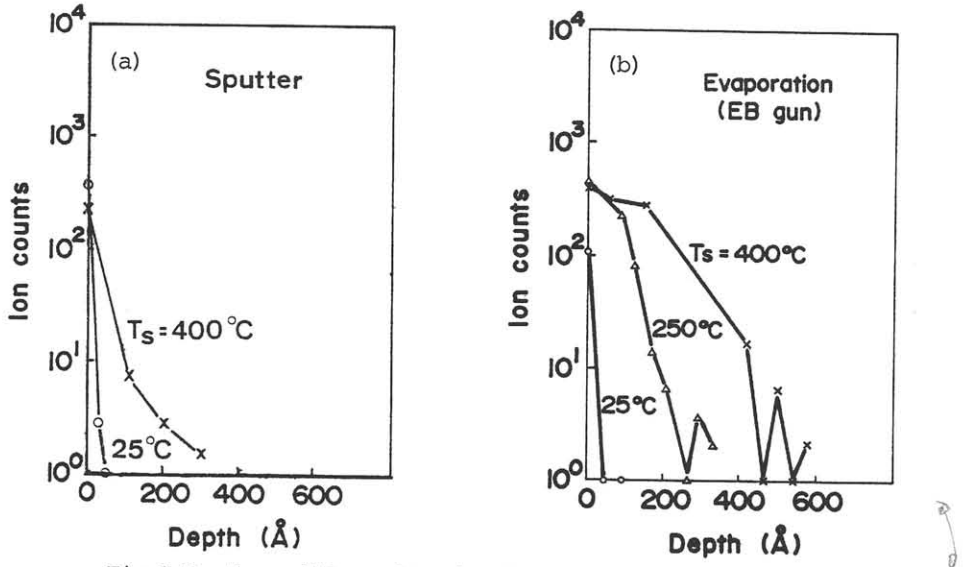

Fig.1 Depth profiles of Mo in SiO_2. Mo films are deposited by sputtering (a) and evaporation (b).

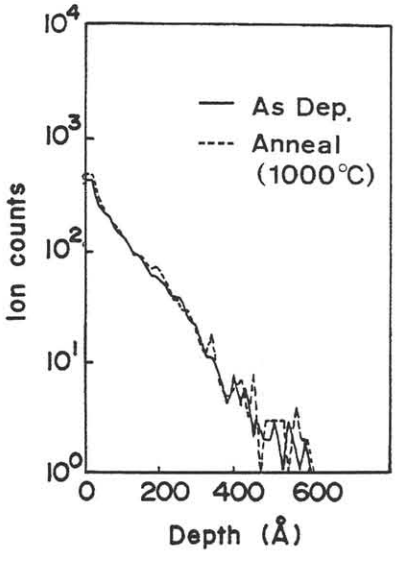

Fig.2 Depth profiles of Mo in SiO_2 before and after annealing at 1000°C.

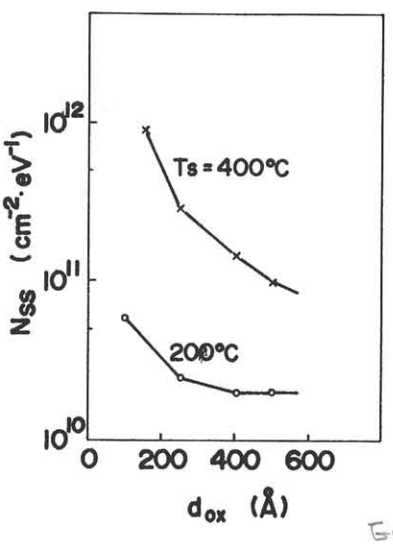

Fig.3 Gate oxide thickness dependence of surface state density.

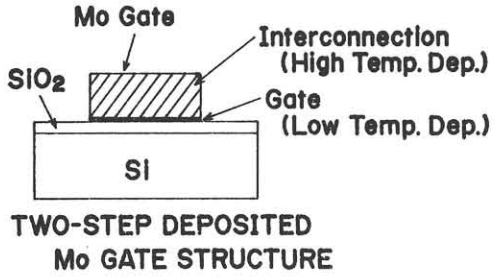

Fig.4 Mo gate MOS structure prepared by the two step deposition method.

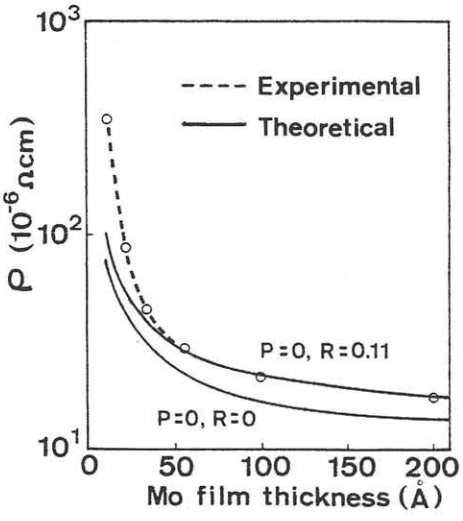

Fig.5 Film thickness dependence of Mo film resistivity.

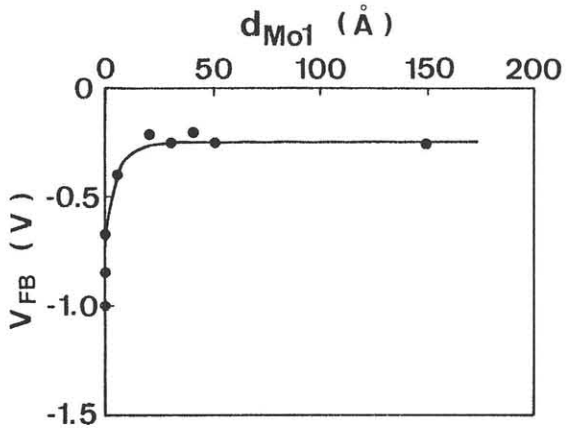

Fig.6 Relationship between flatband voltage V_{FB} and first layer Mo thickness d_{Mo1} of the two step deposition method.

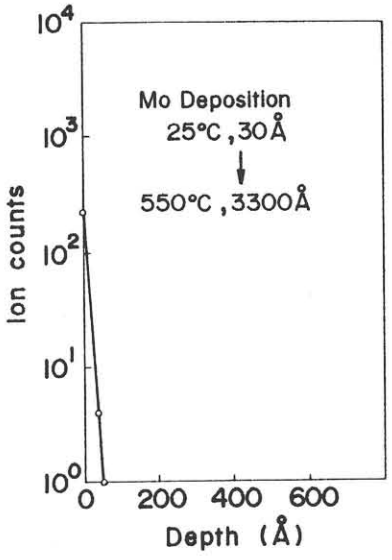

Fig.7 Mo profile in SiO_2 for the two step deposition method.

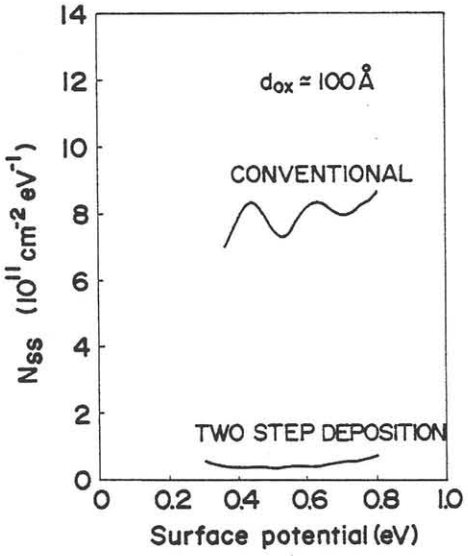

Fig.8 Surface state density of Mo gate MOS diode with a gate oxide thickness d_{ox} of 100 Å.