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MOS Device Characteristics by Perfect Planar Technology

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A new IC fabrication process planarizing for isolation layer through wiring layer (named FLAT) has been developed by planar technology including lift-off technique. Mo stencil and electron cyclotron resonance (ECR) plasma deposition is used for improvements in the conventional lift-off process. Using this technology, a very small step height within 0.2 μm and bird's beak free structure have been achieved. The interface characteristics for the field isolation region, which consists of ECR plasma deposited SiO_2 and Si substrate, show almost the same interface state density as the thermally oxidized SiO_2-Si system. The nMOS FET characteristics are consistent with those fabricated by conventional process except for ß value, which is superior because of bird's beak free structure.

Introduction

As the device structure becomes finer, and the number of metallic layers increases, the surface step coverage and pattern size uniformity should be improved to prevent open and short circuit failures in LSIs. It is difficult to satisfy such requirements by applying conventional techniques to the topography of conventional LSIs.

The Full Leveled Accumulation Technology (FLAT) has been developed by using a new lift-off technique to obtain a flat device surface. The refractory metal (Mo) stencil and the electron cyclotron resonance (ECR) plasma deposition method are employed for the lift-off process. The refractory metal is desirable for a lift-off process stencil to prevent contamination due to residual stencils during high temperature treatment. The ECR plasma deposition method is suitable for the lift-off process, because of its directional deposition property and high quality (1),(2). The perfect planar technology (2) for planarizing multi-level interconnections with high reliability and high yield were previously reported. This paper reports the FLAT applied to an nMOS LSI for planarization in field isolation and gate electrode in addition to multi-level interconnections.

Fabrication Process

The processing steps of field isolation are diagrammatically shown in Fig. 1: (a) A steep side wall consisted of Mo stencil, Si_3N_4 and Si substrate is formed by anisotropic etching in sequence. Boron ions are implanted using the Mo pattern as a mask. (b) The Si trenches formed by the etching are buried with SiO_2 using ECR plasma deposition followed by lift-off technique. (c) The remaining V-grooves are filled by LPCVD poly-Si (or LPCVD SiO_2) after thermal oxidation of the V-groove Si surface. (d) The poly-Si is thermally oxidized using the nitride as an oxidation mask. The oxidized poly-Si layer is etched back in buffered HF solution, leaving poly-Si filled in V-grooves. A capping oxidation follows to the etchback, again using the nitride as an oxidation mask.

In this process, the Mo stencil and ECR plasma deposition method are remarkable features.

Mo stencil

Mo film as a stencil was evaporated at substrate temperature of 250°C using an electron beam gun. A Mo stencil process was established by fine etching techniques and great dissolution rate of Mo in lift-off step. The formations of Si trench ($Mo/Si_3N_4/Si$) and gate electrode

(Mo/poly-Si on SiO_2) are realized by continuous etching techniques. Problems in these etching are pattern forming accuracy and steep side wall formation. So as to obtain steep side walls of these structure, directional etching with very small undercutting for Mo and Si materials were achieved in addition to sufficient selectivity to substrates and etching masks. Etching conditions and characteristics using parallel plate type plasma etchers are summarized in Table 1.

In this lift-off process, Mo is dissolved in H_2O_2-H_2SO_4 mixture. Typical results of the mixing experiment are ploted as Mo lateral etching length vs. time at constant temperature in Figure 2. Mo is not dissolved by H_2SO_4 even at 130°C, while Mo is dissolved by H_2O_2. As shown in Fig. 2, the Mo etching rate is rapid initially, since then, becomes proportional to etching time. The Mo etching length for 5 minutes is more than 100 μm in the solution with H_2SO_4/H_2O_2=1/2 ratio. This etching rate is great enough for the lift-off process.

ECR Plasma Deposited Film

The ECR plasma deposited SiO_2 has such features as high directionality and high quality. The film formed on the side wall can be completely removed in dilute HF solution without erosion of SiO_2 deposited on the flat surface, since the etching rate of the film on the side wall is ten or more times larger than that on the flat surface.

For surface flatness improvement, it is important to minimize the V-groove width, which depends on the thickness of a film formed on the side wall. Reduction of width and depth of V-grooves was obtained by repeating slight etching during ECR film deposition. Figure 3 shows the shape changes of remaining V-grooves with the repetition times for burying Si trenches with 1 μm depth and 2 μm width. With the repetition of 3 times, the maximum width of V-grooves, which is defined at the top, decreases to about 0.25 μm and the depth decreases from 1 um to about 0.85 μm. This result means that even field isolation width below 1 μm can be achieved by this technology.

The interface state density between the deposited plasma CVD SiO_2 film and Si substrate is the most important problem to be overcome in the present technology. To reduce the density, the effect of ECR plasma treatment, employing O_2 gas, was studied. Figure 4 shows the distributions of the interface state density for with and without O_2 plasma treatment (the gas flow rate of O_2 10cc/min for 2 minutes at 100W microwave power). The density is about 3×10^{11} $cm^{-2}eV^{-1}$ at midgap for O_2 plasma treatment, which is below a half of the density for without O_2 plasma treatment. This result is almost the same as that for the wet-oxidized SiO_2-Si interface. From this result, the ECR plasma treatment employing O_2 plasma is confirmed to enable obtaining a clean Si surface without Si surface damage.

Device Characteristics

Test devices were fabricated using the planarization process for gate electrode and multi-level metallization in addition to field isolation. Figure 5 shows a SEM micrograph of fabricated nMOS device cross sectional view having a 1 μm Si trench depth, a 50 nm gate oxide thickness, a 0.45 μm poly-Si gate thickness, a 0.5 μm PSG thickness and a 1 μm thickness for the first Al. Step height for every layer is within 0.2 μm. As is seen in the figure, the bird's beak scarcely appears in the field isolation structure.

Figure 6 shows the threshold voltage for nMOS FET as a function of the channel width. Boron dose implanted for channel cut were 6×10^{13} cm^{-2}, which was not optimized but selected to the same dose as the LOCOS process. Threshold voltage increases as channel width is reduced, which is the similar tendency with the LOCOS process. In the device simulation of this field isolation structure without channel cut borons, however, the threshold voltage decreases as channel width is reduced, contrary to the present result. Therefore, the narrow channel effect of this work results from lateral diffusion of borons in the field perimeter. The boron dose for channel cut must be optimized to a lower value, to reduce the narrow channel effect.

Device parameters and characteristics for nMOS FETs are summarized in Table 2. The substrate bias sensitivity and drain bias sensitivity for

threshold voltage are very close to the results for LOCOS structure. ß, which is proportional to the channel width, carrier mobility and gate capacity and in inverse proportion to the channel length, is 1.5 times larger than that for LOCOS structure. The difference between the effective channel width and mask dimension is 0.5 μm for this work and 1.5 μm for LOCOS, respectively. This result is due to the directional etching of Si trench and bird's beak free structure. The gate bias sensitivity of subthreshold current is consistent with the LOCOS results. This result means that the lateral diffusion of boron for channel cut eliminates the side wall channel leakage current.

Conclusion

The Full Leveled Accumulation Technology (FLAT) for nMOS LSIs using lift-off technique has been developed. A very small step height, within 0.2 μm, and bird's beak free structure with no channel leakage current has been realized. The Mo stencil process and ECR plasma deposition method show sufficient properties for improvements in lift-off process. ECR O_2 plasma is used to reduce the interface state density between ECR plasma deposited SiO_2 and Si substrate. The MOS FET characteristics are consistent with those fabricated by conventional process except for ß value, which is superior because of reduction of difference between dimension on mask and effective channel width.

Acknowledgement

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References

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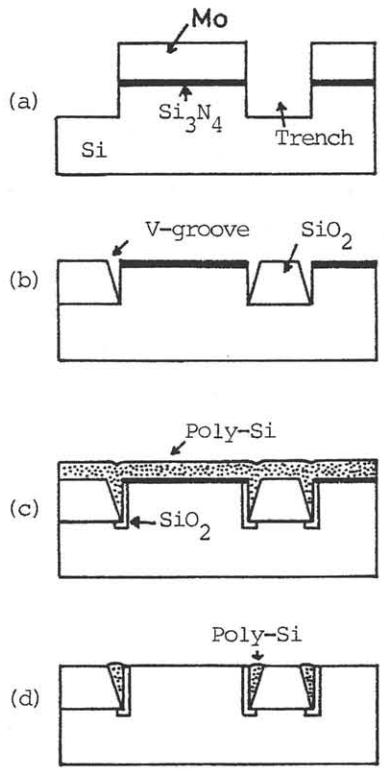

Figure 1.
Field isolation process sequence.

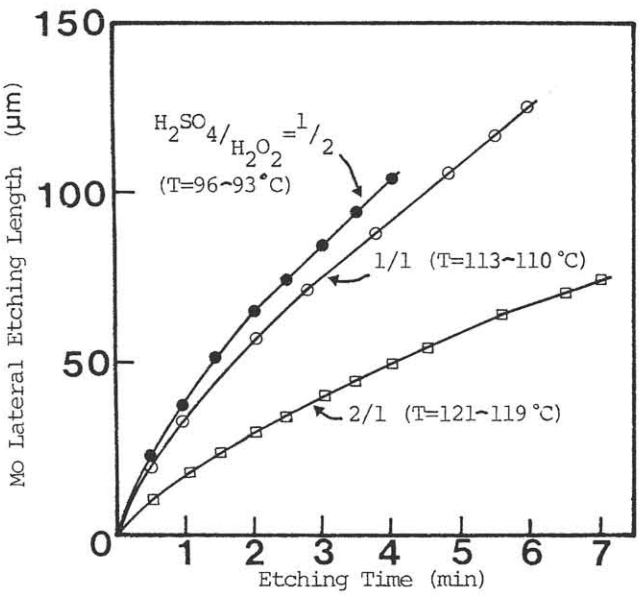

Figure 2
Mo etching length as a function of etching time with H_2SO_4/H_2O_2 ratio as a parameter, where T is the temperature of solution.

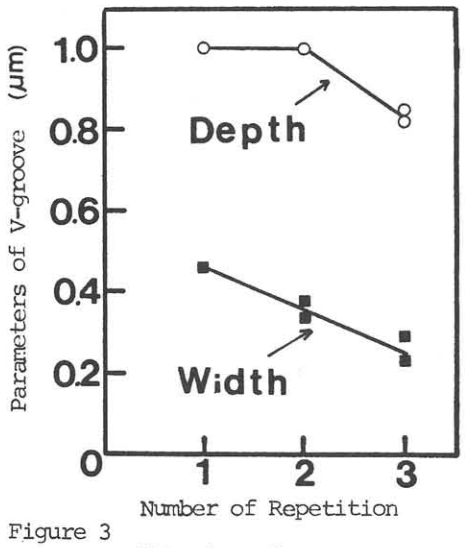

Figure 3
V-groove profile dependence on repetition times for burying 1 μm trench with ECR plasma deposited SiO_2.

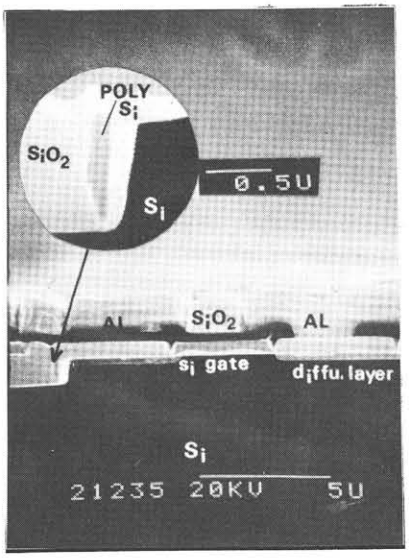

Figure 5
SEM micrograph of a cross section of nMOS device.

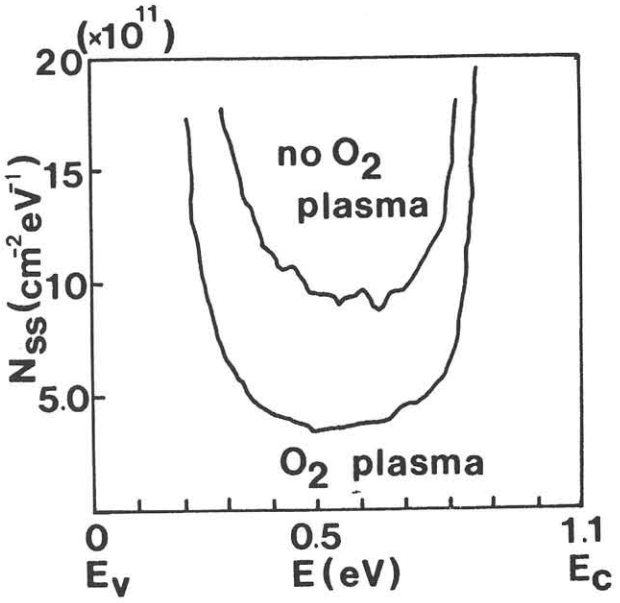

Figure 4
Interface state density in ECR plasma deposited SiO_2.

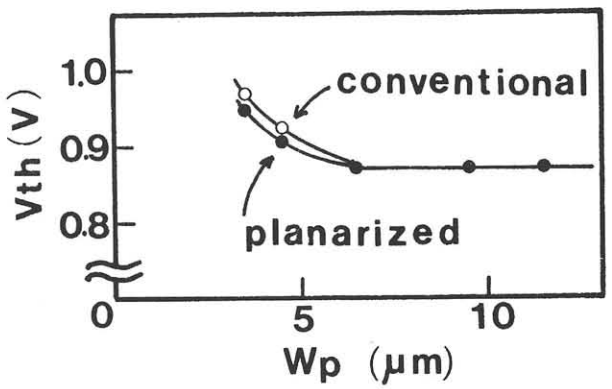

Figure 6
Threshold voltage versus channel width on mask pattern.

Table 1 Etching conditions and characteristics

Material	Etching Gas	Substrate	Etching Mask	Etching Rate Ratio		Undercutting (both side)
				To Substrate	To Mask	
Mo	CCl_4+O_2	undoped poly-Si	AZ resist	15	5	0.1 μm
Si	$CBrF_3+O_2$		AZ resist + Mo		4	0.1 μm
undoped poly Si	CCl_4	SiO_2	AZ resist + Mo	more than 50	20	0 μm

Table 2 Device parameters and characteristics

	Planarized	Conventional
Effective channel length	2 μm	2 μm
Channel width on mask	3.5 μm	3.5 μm
Substrate bias sensitivity	0.19	0.19
ß	72 μmhos/V	49 μmhos/V
Drain bias sensitivity	0.01	0.01
Subthreshold swing	85 mV/decade	85 mV/decade