

## A Very Small "Super-8" Size CCD Image Sensor

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Solid state image sensors have received increasing attention as alternates to pick-up tubes for small portable video cameras. Majority of electron-beam tubes have recently been miniturized from 2/3 to 1/2 inch size for reduction of the camera size. On the other hand, the image format in the conventional solid-state imagers, either CCD<sup>1)</sup>, MOS<sup>2)</sup>, or CPD<sup>3)</sup> configuration, has been of 2/3 inch size so far, which requires the chip area as large as 100 mm<sup>2</sup>.

This paper describes a very small size 490(V) x 404(H) element interline CCD image sensor compatible to the "Super-8" movie lenses. The chip size is less than one half of that of the conventional 2/3 inch image sensors.

Fig. 1(a) and (b) show the schematic configuration of the image sensor and the cross-sectional view of the unit cell, respectively. The cell consists of one photodiode (PD), one-half stage of a 4-phase buried channel vertical shift register (V.BCCD) including a threshold controlled transfer gate region (TG). For blooming suppression, the two level p-well structure<sup>1)</sup> is utilized. The photodiode is made in a shallow, lightly doped p-layer, while the rest of the cell is formed in a thick, highly doped p-well. The n-type substrate is reversely biased by  $V_{SUB}$  from the grounded p-well. The excess charge overflows through the lightly doped p-layer into the n-type substrate to eliminate blooming, while the rest of the p-well region in the cell is kept undepleted. The unit cell size is 8.8  $\mu\text{m}$ (V) x 15.1  $\mu\text{m}$ (H). The channel width of the V.BCCD is designed as 5.5  $\mu\text{m}$  considering the high charge handling capability and the high transfer efficiency. The output amplifier is constructed with the floating diffusion of two-stage source follower, and the signal charge is read out using correlated double sampling to reduce 1/f noise. The floating diffusion sensing capacitance is minimized as small as possible to reduce kTC noise.

The device was fabricated on an 8-12 $\Omega$ -cm n-type silicon substrate using the double-layer polysilicon technology and the 2  $\mu\text{m}$  rule fine pattern process with boron implantation for the p-well formation. In order to make the channel depth as shallow as possible, arsenic ions were implanted for the V.BCCD.

Figure 2 is a photograph of a fabricated image sensor. The chip size is 5.68 mm(V) x 7.12 mm(H). The imaging area is 4.32 mm(V) x 5.73 mm(H), which is smaller than the 1/2 inch size and compatible to the "Super-8" movie format.

The signal-to-noise ratio obtained is 60 dB at the saturation level. The saturation current is 200 nA, which is determined by the charge-handling capacity of the photodiode.

Figure 3 shows a reproduced image from a resolution chart together with a tungsten lamp. It is seen that horizontal and vertical resolution values are 280 TV lines and 480 TV lines, respectively, and blooming and smearing are fairly suppressed.

A single chip color camera using the present "Super-8" size image sensor has been implemented. The color filter is composed of mazenata, cyan, yellow, green<sup>4)</sup>. The signal-to-noise ratio in the field integration mode operation<sup>4)</sup> was 55 dB under a scene illumination level of 300 lx (F1.4), which is 50% of the saturation illumination. These imager characteristics obtained are sufficiently suited for application in small video cameras.

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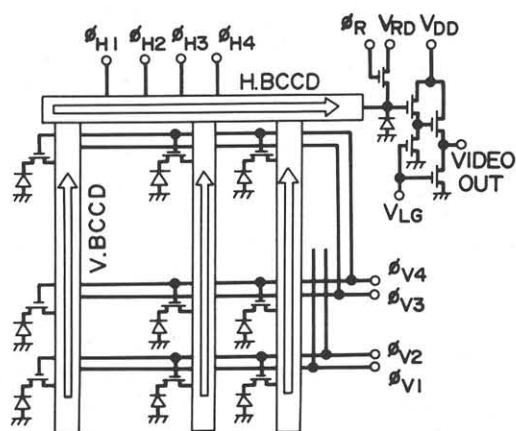


Fig. 1 (a) Schematic configuration of the image sensor

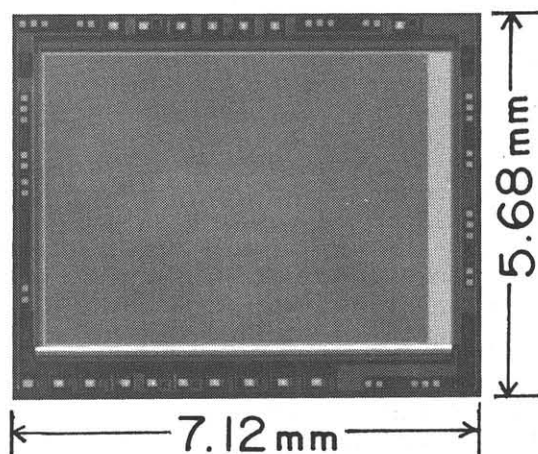


Fig. 2 Photograph of the image sensor

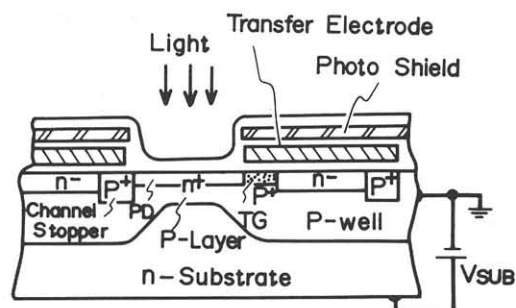


Fig. 1 (b) Cross sectional view of a unit cell

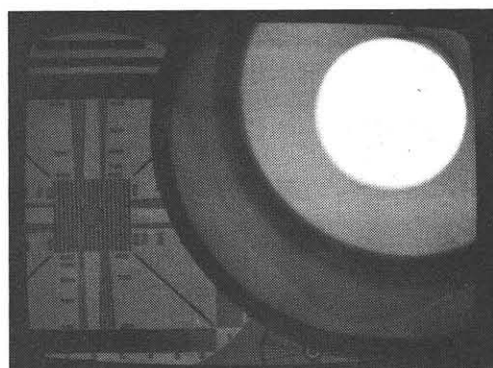


Fig. 3 An image reproduced by the image sensor