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Depletion Trench Capacitor Cell

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Depletion trench capacitor(DTC) cell technology has been developed for future megabit dRAMs. Its purpose is to increase cell capacitance without increasing cell size and to reduce the effect of supply voltage fluctuations on dRAM operation. Cross sectional rectangular trenches were successfully formed by RIE using $CBrF_3$ gas. Phosphorus was doped onto the trench surface by diffusion from phospho-silicate glass film. The electrical characteristics of DTC are sufficiently good for practical application under a 3V operating condition. DTC with 15nm capacitor oxide was applied to a submicron CMOS 256Kb dRAM and was confirmed to be applicable to future megabit dRAMs.

I. INTRODUCTION

In the development of a megabit level MOS dRAM, cell capacitance deficiency has become one of the most serious problems because of the requirement for cell size reduction. Further reduction in the thickness of the capacitor oxide will soon not be feasible from the reliability standpoint. Thus, new ways to increase the cell capacitance are now greatly needed.

We have proposed a depletion trench capacitor (DTC) cell technology, in which a depletion type capacitor is formed in a trench[1,2]. Its purpose is to increase the cell capacitance without increasing cell size and to make possible the operating of a dRAM with a cell plate bias voltage of 0V. A corrugated capacitor cell(CCC), reported on by H. Sunami et al.[3], is a similar technology, but which does not include depletion capacitor technology. We have also reported on a submicron CMOS 256Kb dRAM fabricated by utilizing DTC[4].

In this paper, DTC technology and its application to a submicron 256Kb dRAM are described.

II. ASSUMPTIONS BEHIND DTC DESIGN

We assumed the following conditions in order to confirm the applicability of DTC to megabit level MOS dRAMs.

The operating voltage is 3V so as to reduce the threshold voltage shift of submicron channel length MOSFETs due to hot-electron injection. The cell plate bias is 0V so as to decrease the effect of supply voltage fluctuation on the memory operation.

III. PROCESS SEQUENCE

CZ-P type (100) silicon substrates of 4-5 ohm-cm are used. The DTC process sequence applied to 256Kb dRAM fabrication is shown in Fig. 1.

(1) A field oxide is formed by using the conventional local oxidation process, and then n-type layers are formed in the cell capacitor region (plane surface) by phosphorus ion implantation.

(2) Trenches are formed by reactive ion etching(RIE) using $CBrF_3$ gas, where CVD SiO_2/ Si_3N_4/pad SiO_2 layers are used as etching masks. Then, trench surface layers are slightly wet etched.

(3) Phospho-silicate glass(PSG) is deposited by atmospheric-pressure CVD. Phosphorus is then diffused onto the trench surface layers.

(4) Following the removal of the PSG film and the etching mask layers, a gate oxide film is thermally grown. The trenches are filled with low-pressure CVD polysilicon which is used as a cell plate electrode.

IV. KEY PROCESS TECHNOLOGIES

(1) Trench formation

$CBrF_3$, $CClF_3$, and CCl_2F_2 were studied as Si etching gases for RIE. RIE using low pressure $CBrF_3$ gas was found to be the best for forming trenches with a rectangular cross sectional shape[5]. SEM micrographs of trench cross-sections are shown in Fig. 2, where RIE was performed using $CBrF_3$ under the condition that gas pressures were 14 mtorr and 20 mtorr and etching power density (P_E) was 0.09 W/cm^2. The gas pressure of 14 mtorr was found to be preferable and P_E had little effect on the trench shape. On the other hand, it was found that P_E greatly influenced the formation of contaminated and/or damaged layers. From the observation of oxidation induced stacking fault (OSF) density on a Si surface etched at P_E=0.09-0.36 W/cm^2, it was shown that OSF density increased with an increase in P_E. To remove contaminated or damaged layers, trench surface layers of 50 nm were etched in a mixture of HNO_3, CH_3COOH, and HF. Trench capacitor leakage current is improved by this slight wet etching as shown in Fig. 3, when P_E=0.09 W/cm^2.

(2) Phosphorus doping onto trench surface

Phosphorus concentration(Ns) at the trench surfaces in DTC formation is restricted within the range of from about 5×10^{17} cm^{-3} to 1×10^{19} cm^{-3}. The minimum Ns is derived from the requirement that the inversion layers be formed under the cell plate even when the bit lines are in a high level. Maximum Ns is limited by the requirement that no enhanced oxidation occur in the gate oxidation process[6].

For the plane surface, the relation between the PH_3/SiH_4 flow ratio and Ns is shown in Fig. 4(a). The scattering of Ns was less than 30% above a PH_3/SiH_4 flow ratio of 2%. The relationship between PSG thickness(t_p) and Ns is shown in Fig. 4(b). Ns as a function of t_p has a maximum value at t_p=0.2-0.3 μm. It is thought that the decrease in Ns for PSG film thicker than 0.3 μm is caused by suppressed diffusion due to film stress and that the decrease in Ns for PSG film thinner than 0.2 μm is caused by source phosphorus insufficiency.

To examine the controllability of Ns at the trench bottom, the threshold voltages of trenched ring gate MOSFETs are measured. A cross-sectional view of the MOSFETs structure is shown in Fig. 5. Trench width dependence of the threshold voltage(Vth) and the ratio of the trench bottom PSG thickness to plane surface PSG thickness are shown in Fig. 6. The solid line in Fig. 6 represents computer simulation results of the Vth in which Ns dependence on PSG thickness shown in Fig. 4(b) is taken into account. Since the simulation results closely agrees with the measured ones, it is found that Ns dependence on PSG thickness at the trench bottom is the same with that at the plane surface. This means that Ns can be controlled at the trench bottom as well as at the plane surface.

By taking account of these experimental results, the phosphorus doping conditions were decided. These were a PSG thickness of 0.3 um, a PH_3/SiH_4 flow ratio of 2%, and phosphorus diffusion at 1000°C for 1 hour.

(3) Trench filling with polysilicon

The polysilicon thickness in the trenches was the same as that on the plane surface. Trenches could be completely filled with polysilicon whose thickness was greater than one half of the trench width. An SEM micrograph of the trench cross-section following polysilicon filling is shown in Fig. 7.

V. TRENCH CAPACITOR CHARACTERISTICS

The capacitance of trench capacitors was measured. Trench patterns were rectangular and parallel in the [110] direction. The relationship between the capacitance and the trench sidewall area as well as the trench bottom area is shown in Fig. 8. The capacitance per unit area at the sidewall is about 30% smaller than that at the plane surface. This is probably due to the surface orientation difference between the (110) sidewall and the (100) plane surface, since the oxidation rate of the (110) surface is about 30% larger than that of the (100) surface[7].

Breakdown voltage histograms for DTCs as well as depletion plane capacitors(DPCs) are shown in Fig. 9. The breakdown voltages of DTCs are smaller than those of DPCs. The breakdown voltage degradation is considered to be caused by the localized thinning of gate oxide at the sharp trench edges[8]. For the practical application of DTC, no problems will arise from the standpoint of

breakdown voltage degradation. The reason for this is that the leakage current is sufficiently small at a gate voltage of 3V.

VI. APPLICATION TO A SUBMICRON CMOS 256KB DRAM

DTC was applied to a submicron CMOS 256Kb dRAM. An SEM micrograph of DTC cells is shown in Fig. 10. The trench size is 0.5 μm in width, 3.5 μm in length and 1.5 μm in depth. The capacitance of the DTC cell was estimated to be 40 fF, which is 20 fF larger than that of the DPC cell.

The holding time of the RAM with DTC cells was 500 msec and that of the RAM with DPC cells was 100 msec at room temperature. This difference is considered to be caused by the storage charge difference between the DTC cell and the DPC cell. From this result, it was confirmed that DTC technology is applicable to future megabit level dRAMs.

ACKNOWLEDGEMENTS

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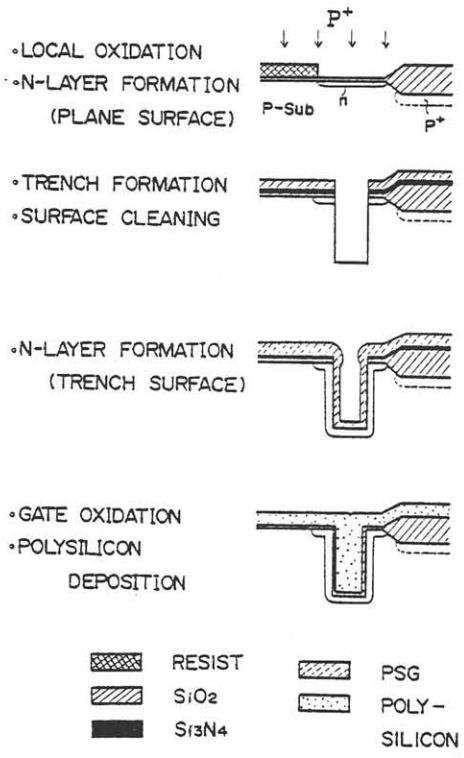


Fig. 1 DTC process.

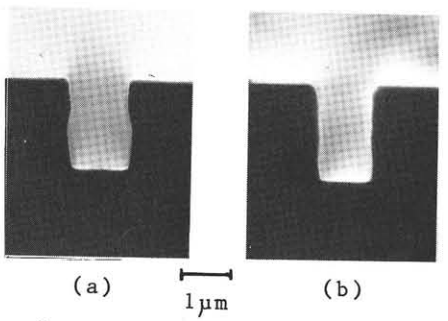


Fig. 2
SEM micrographs of trench etched under 20 mtorr (a) and 14 mtorr (b) with $CBrF_3$.

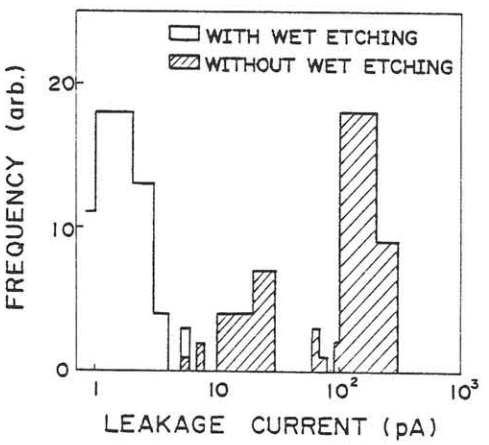
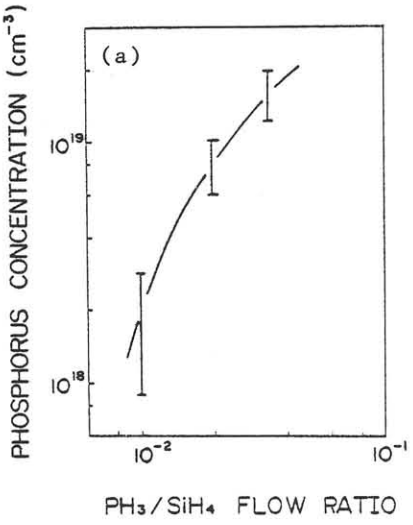


Fig. 3
Histograms of trench capacitor leakage current at 7V. The oxide thickness is 20nm.



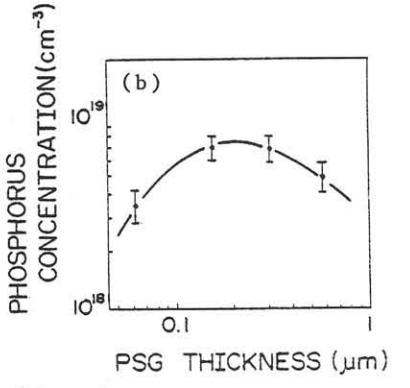


Fig. 4
Dependence of phosphorus concentration at Si surface on PH_3/SiH_4 flow ratio at PSG deposition (a) and that on PSG thickness (b).
Phosphorus was diffused at 1000°C for 1 hour in N_2.

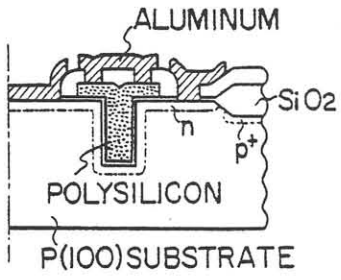


Fig. 5
Cross-sectional view of MOSFET structure with trench.

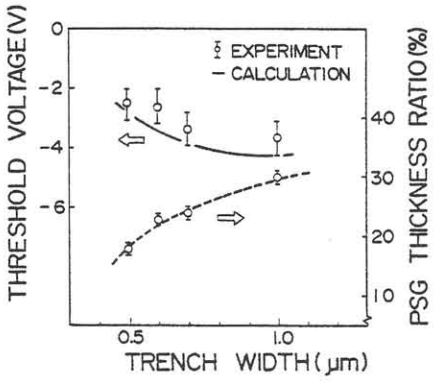


Fig. 6
Threshold voltage of MOSFETs and PSG thickness ratio on bottom/plane surface as a function of trench width.

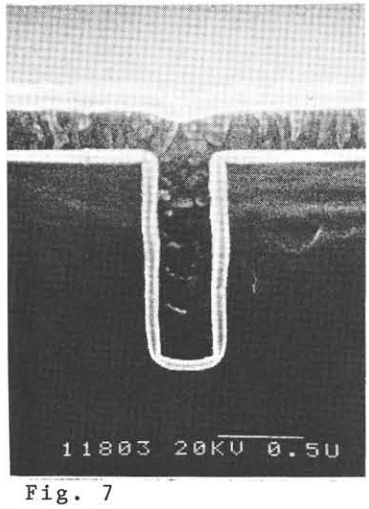


Fig. 7
SEM micrograph of DTC cross section.

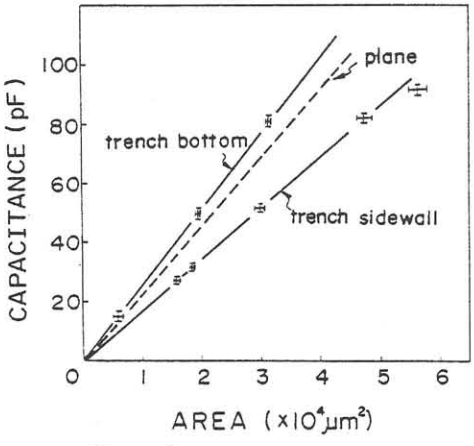


Fig. 8
Relationship between capacitance and trench sidewall, trench bottom, as well as plane surface areas.

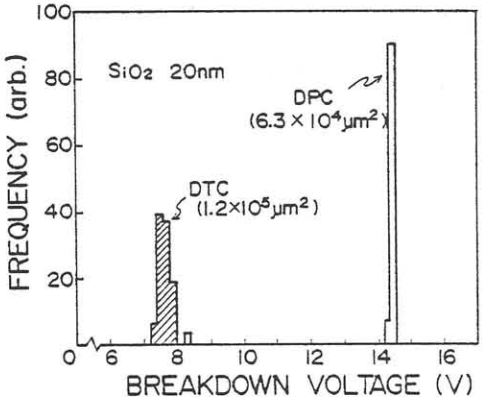


Fig. 9
Breakdown voltage histograms for DTCs and DPCs.

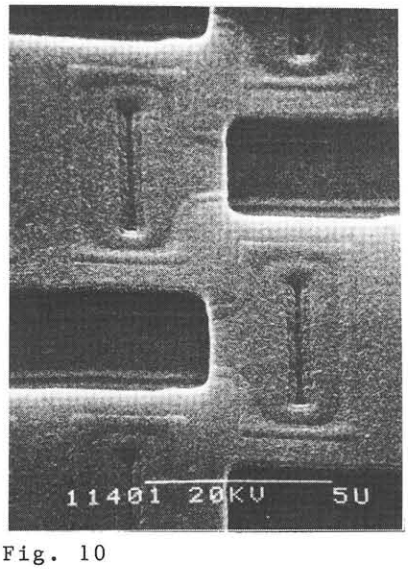


Fig. 10
SEM micrograph of DTC cell after the polysilicon patterning.