Extended Abstracts of the 15th Conference on Solid State Devices and Materials, Tokyo, 1983, pp. 261-264

A-7-4

The Impact of Drain Impurity Profile and Junction Depth on Submicron MOSFETs

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A re-examination of the influence of drain impurity profile and junction depth on submicron MOSFETs has been made from the viewpoint of short-channel effects, transconductance degradation, and hot-carrier-related device degradation using 2-D simulation (SUPREM and CADDET) and experiments. It is shown that little scaling or even up-scaling of junction depth, rather than the simple down-scaling proposed by Dennard, improves both short-channel effects and hot-carrier effects in the submicron regions. Also, using the gaussian junction as the drain impurity profile is important. Thus, from this finding, significant guiding principles for device scaling in the realization of sophisticated submicron MOSFETs are proposed.

§1. Introduction

Short-channel effects and hot-carrier effects are obviously the most pressing problems in realization of sophisticated submicron MOS VLSIs. They also seem to have a design trade-off relationship. However, it is necessary to alleviate both effects at the same time. Recently, such device structures as double-diffused drain(DDD)[1] and lightly doped drain(LDD),[2] both of which make use of drain-shape modulation techniques, the so-called "Drain Engineering", have been proposed to improve device reliability. It has been found, however, that these structures cause reduced drive capability or degraded V_{th} lowering.[3-4]

In this paper, a re-examination of the influence of drain impurity profile and junction depth on MOS devices with submicron dimensions is made from such an overall viewpoint as V_{th} lowering, transconductance degradation, and hot-carrier induced device performance degradation, using both 2-D simulation(SUPREM[5] and CADDET[6]) and experiments.

Although it has been commonly accepted in scaling theory[7] that junction depth, x_j, should be scaled with the same scaling factor as other device dimensions, it is shown here that little scaling or even up-scaling of x_j, rather than simple down-scaling, is important in reduction of both short-channel and hot-carrier effects in submicron regions. It is also necessary to use the gaussian junction as the drain impurity profile.

This gaissian profile has the useful role of moving the peak position of the electric field near the drain into the Si-substrate, both vertically and horizontally, as well as reducing the electric field strength.

§2. Experimental

In parallel with 2-D simulation, experiments were carried out to the simulated results. The MOS devices used consist of an As drain for the nearly abrupt junction and As-P double drain[8] as the nearly gaussian junction. Effective channel length, L_{eff}, was varied from 0.5 to 5 μm. Gate oxide thickness was 20 nm. Gate material was polysilicon. Junction depth, x_j, was 0.2 - 0.45 μm. The final passivation layer was silane. All data was taken at room temperature.

§3. Results and discussions

A. V_{th} Lowering

Figure 1 shows a comparison of V_{th} lowering characteristics between abrupt and gaussian junctions for MOS devices with T_{ox} = 20 nm, with x_j as a parameter. This figure shows that V_{th} lowering becomes more remarkable with increased x_j in the case of the abrupt junction, while, for the gaussian junction, V_{th} lowering hardly degrades at all, and, to the contrary, for x_j = 0.6 μm with L_{eff} = ~0.5 μm, it is rather improved. These simulation results are more explicitly demonstrated in Fig. 2, which shows V_{th} lowering ratio to effective channel length as a function of x_j. In the case of the

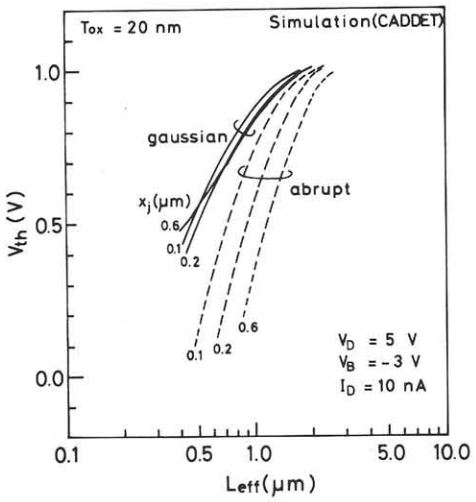

Fig. 1. V_{th} lowering characteristics for both abrupt and gaussian junctions.

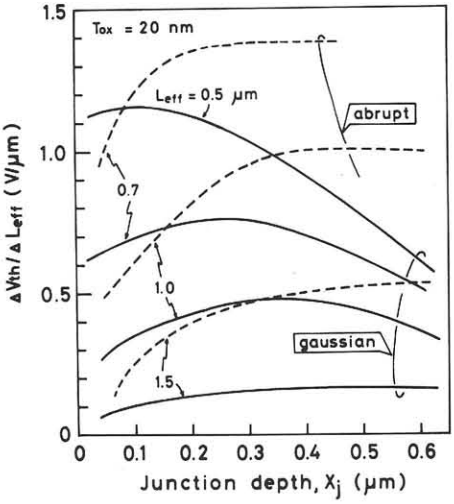

Fig. 2. V_{th} lowering ratio to L_{eff} variation for both abrupt and gaussian junctions as a function of junction depth.

abrupt junction, the ratio increases monotonically, as expected, with the increase in x_j. On the other hand, for the gaussian junction, the ratio decreases at any x_j larger than 0.2 - 0.3 μm in the region of $L_{eff} \leq 1$ μm. Such a peculiar tendency becomes more remarkable in submicron regions.

These interesting results can be explained in terms of surface potential in the channel, as shown in Fig. 3. It should be pointed out that, in the case of the gaussian junction, the maximum potential position move horizontally further into the drain junction as x_j increases, while, for the abrupt junction, it is fixed at the edge of the drain junction, and the minimum surface potential position in the center of the channel increases, which leads to degraded V_{th} lowering. Therefore, the gaussian junction is found to substantially increase the effective channel length and improve V_{th} lowering characteristics.

These simulation results are also proven by experiments using phosphor(P), which provides a nearly gaussian profile, as a drain diffusant. Figure 4 shows the experimental results of V_{th} lowering for MOS devices with an As-P double drain. Arsenic(As) was used to reduce resistivity in the diffusion layer. It is found that, as predicted by simulation, As-P drain MOS devices show little dependence of V_{th} lowering on junction depth, and at x_j = 0.45 μm, V_{th} lowering even seems to become weak in the region $L_{eff} \leq 0.5$ um.

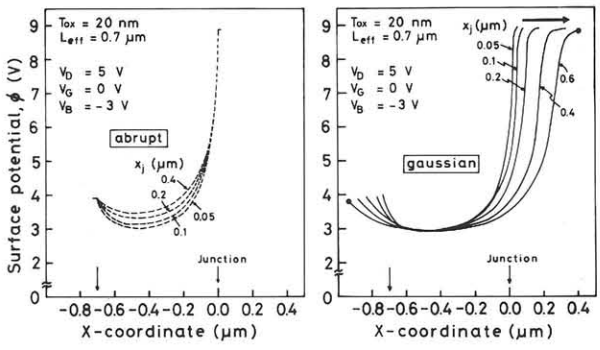

Fig. 3. Comparison of surface potential between devices with abrupt and gaussian junctions.

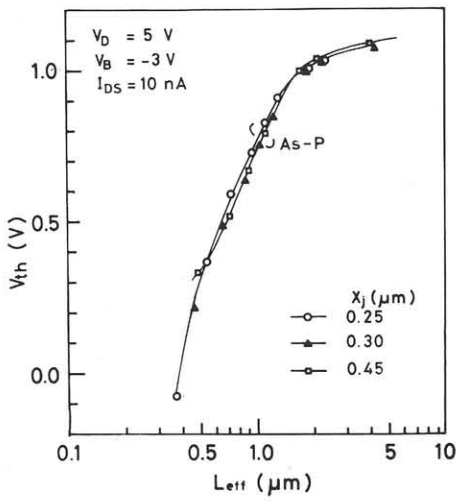

Fig. 4. Experimental V_{th} lowering characteristics for As-P devices, with x_j as a parameter.

B. Transconductance(G_m) Degradation

Due to the substantial increase in L_{eff}, slight G_m degradation occurs in the case of the gaussian junction with increased x_j, compared to that for the abrupt junction. Figure 5 shows the x_j- dependence of transconductance, with L_{eff} as a parameter. It should be noted that, although the transconductance gradually decreases with increased x_j, in the gaussian junction, it decreases, at most, 8 - 9 % in a MOS device with L_{eff} = 0.5 μm and x_j = 0.3 μm. This is because the gate electrode covers the drain diffusion layer, which leads to lessening of the increase in its diffusion resistance. In the LDD structure,[4] however, the lightly doped off-set diffusion layer, on the other hand, acts as a resistance. The G_m - x_j relationship thus obtained is useful when optimizing x_j in submicron regions.

C. Hot-Carrier Effects

The influence of drain impurity profile is also remarkable in terms of hot-carrier effects. Figure 6 shows the position of the maximum electric field within a device and the electric field along the Si surface for both abrupt and gaussian junctions. While the maximum electric fields and their positions have little dependence on x_j and are fixed at the drain edge in the case of the abrupt junction, for the gaussian junction the maximum electric field position moves further into the Si-substrate from the Si-surface, and the electric field also decreases with increased x_j. In particular, the fact that the maximum electric field position, where most of the hot-carriers are generated and injected into the gate-oxide, move into the Si-substrate is very significant for reducing hot-carrier effects. This can be by considering that hot-carrier injection ratio, P,[9]

$$P = A \exp(-d/\lambda); \quad A = 2.9 \ldots\ldots\ldots (1),$$

where λ is the carrier mean-free-path and d is the distance from the Si-surface. For example, the d at x_j = 0.3 μm in the gaussian junction is about 0.1 μm, while λ is 5 - 10 nm. The effect of d, the so-called "vertical off-set" is considerable.

Figure 7 shows a stress-time variation in G_m degradation under the condition of sustrate current, $I_{BB} = 1.6 \times 10^{-4}$ A (constant), for both As drain and As-P drain MOS devices with L_{eff} = 0.8 μm and x_j = 0.3 μm. It was found that an As-P nearly gaussian junction provides stronger resistance to

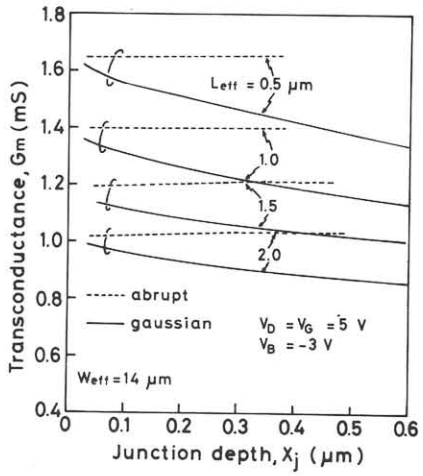

Fig. 5. Transconductance characteristics as a function of x_j for abrupt and gaussian junctions.

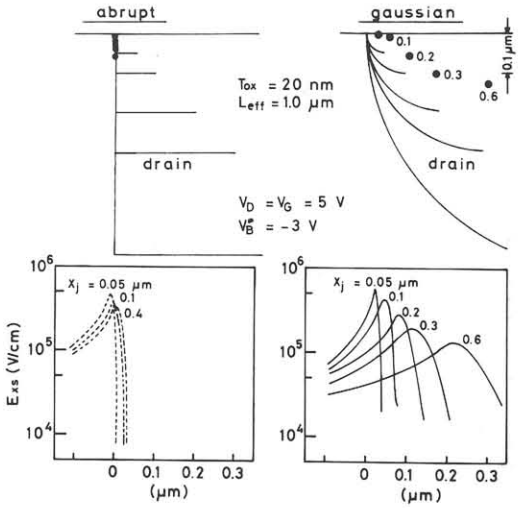

Fig. 6. Maximum electric field position and the electric field along the Si-surface for both abrupt and gaussian junctions.

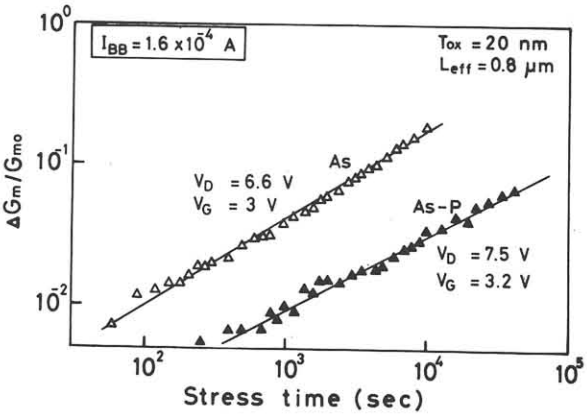

Fig. 7. Stress-time variation in transconductance degradation for both As and As-P drain MOSFETs with L_{eff} = 0.8 μm and x_j = 0.3 μm.

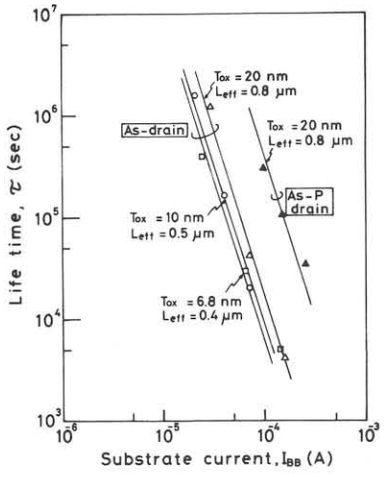

Fig. 8. Lifetime experimentally obtained for both As and As-P drain MOSFETs as a function of substrate current.

hot-carrier-related device degradation, compared with that for an As nearly abrupt junction. It is significant that the stress condition(V_D = 7.5 V) for the As-P drain is more severe than that(V_D = 6.6 V) for the As drain.

Figure 8 compares lifetime, τ , to hot-carrier effects for both As drains and As-P drains as a function of substrate current. The lifetime was defined as the time it takes for V_{th} to shift 10 mV. It is clear from this figure that As-P drains have longer lifetimes, by more than one order of magnitude, than As drains, in spite of the fact that substrate current, which is considered the most important criterion when diagnosing hot-carrier injection, is constant. Constant substrate current also means that the electric field or ionization integral is approximately constant. These experimental results are considered to reflect the above simulation results; i.e., vertical off-set effect.

§4. Conclusion

The influence of drain-shape; impurity profile and junction depth, on submicron MOSFETs for the next generation VLSIs has been examined in terms of short-channel effects, drive capability, and device reliability. On the basis of both experiments and simulation, two guiding principles that are different from simple scaling law[7] for reducing short-channel and hot-carrier effects in terms of drain profile and junction depth have been obtained:

1) Use a gaussian impurity profile, and
2) Do not scale the junction depth in proportion to other dimention scaling; instead, use an x_j of greater than 0.3 μm, even in the submicron regions.

The rigid value of x_j can be determined by considering the allowable G_m degradation.

The above guidelines are due to both a) the substantial increase in L_{eff} and b) the vertical off-set of the electric field from the use of the gaussian junction and deeper junction depth, as well as reduction of the electric field. These drain engineering technologies should be increasingly important for realization of more reliable submicron MOS devices, regardless of power supply voltage reduction, in the near future.

Acknowledgement

The authors would like to thank Dr. M. Kubo, Dr. H. Kume, and Dr. N. Hashimoto for their helpful discussions. They also thank Dr. A. Shimizu of Hitachi Microcomputer Engineering Ltd. for his support during device fabrication.

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