Extended Abstracts of the 15th Conference on Solid State Devices and Materials, Tokyo, 1983, pp. 273-276

A-7-7

Electron Beam Testing Techniques for Dynamic Memory

Masayuki Sato and Shozo Saito

Semiconductor Device Engineering Laboratory, Toshiba Corporation,

Saiwai-ku, Kawasaki 210, Japan

Newly developed electron beam testing techniques for dynamic memory devices are described. We introduce measuring point shielding technique and optimized beam condition. The local electric field effect and shielding effect are evaluated by measurement of test devices and two dimensional computer simulation. Then, good accuracy is achieved for dynamic memory testing. Utilizing these measuring techniques, the internal timing of a 256k dynamic RAM is measured and compared with circuit simulation waveforms. Consequently, we obtained useful information for optimization of the circuit design of dynamic memory devices.

1. Introduction

Recently, minimum design rules of VLSI memory devices have been scaled down to 1 ~ 2um level to achieve high performance and high bit density. Therefore, a conventional measurement technique using mechanical probes became to be difficult to measure internal timings of VLSI circuits with sufficient accuracy, because a parasitic capacitance of a probe itself is usually much larger than those of internal node and measurement point is small geometry. To overcome this disadvantage, an electron beam tester has been developed and experimentally applied for design verification and failure analysis.[1,2]

This paper describes electron beam testing technique for a newly developed 256k bit dynamic memory[3].

2. Electron beam tester

Fig. 1 shows the block diagram of the electron beam tester used for the dynamic memory testings.[4] System controller sends control signals to LSI tester to operate the LSI device under test and to control the electron beam. Secondary electrons emitted from LSI device surface are detected by photomultiplier tube PMT and stored for subsequent data processing. A time resolution of this system is 1ns. In order to avoid the electron radiation damage and the surface charging of devices, we chose the acceleration voltage of 2kv.

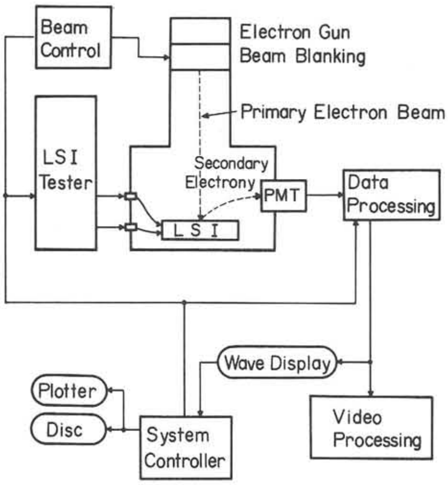


Fig. 1 Block diagram of the Electron Beam Tester.

3. Measurement and discussion

3.1 The local electric field effect

There are two serious problems to measure the internal nodes potential and timings of the dynamic RAM accurately. One is the local electric field effect which comes from the neighboring wiring patterns. The other is the electron beam effect on the internal floating node potential of the dynamic RAM.

To overcome the first problem , we introduced the shield metal technique , which surrounds the measuring point. Fig. 2 shows the measuring metal pattern layout and the detected signal

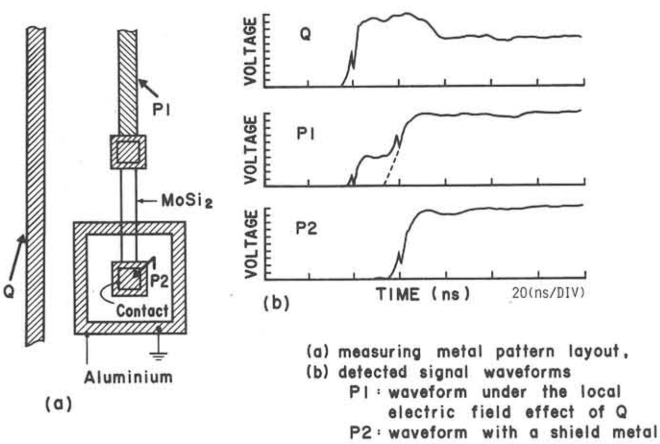
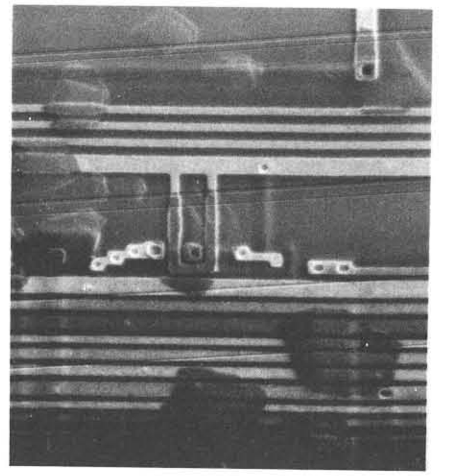
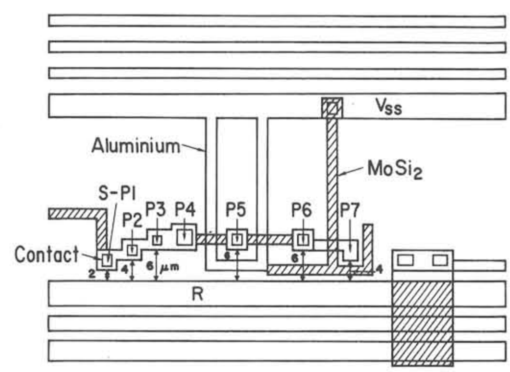


Fig. 2 Comparison of the detected node potential without and with shield metal.



(a)



(b)

Fig. 3 The testing device for evaluating the local electric field effect. (a) A SEM photograph; (b) the pattern layout.

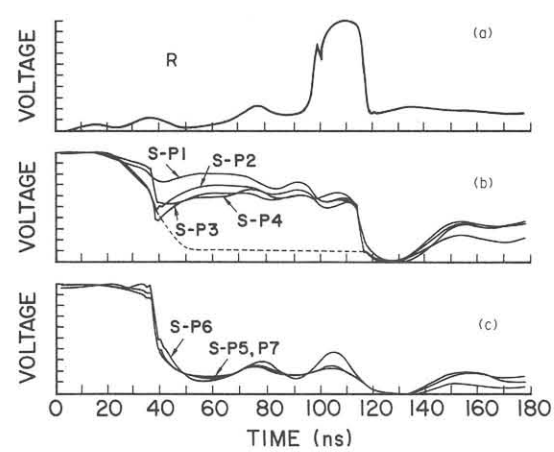


Fig. 4 The detected signal waveforms for the testing device shown in Fig. 3. (a) Waveform of the neighboring line R; (b) Waveform of the measuring line S under the local electric field effect of R; (c) Waveform of S with a shield line (P5: Al, P6: $MoSi_2$).

waveforms. P1 and P2 are measuring point and Q is the neighboring wiring patterns, which have influence upon P1 and P2. It shows that the difference between the detected waveforms at P1 and P2 corresponds to the shield effect.

Now let us consider the quantitative analysis of the local electric field effect by measuring the test device and two dimensional computer simulation. A SEM photograph and pattern layout of this test device are shown in Fig. 3(a) and (b), respectively. In this figure, R is a neighboring pattern which have influence upon several measuring signal S, and S-P1, P2 and P3 are the measuring point by changing the interval of the measuring point of the signal line S and the neighboring pattern R, respectively. Furthermore, P5, P6 and P7 are changed the shield material to investigate the difference of the shielding effect. Fig. 4(a) shows the neighboring pattern signal. Fig. 4(b) and (c) show the detected signal waveforms at several measuring point S-P1 ~ P7. In Fig. 4(b) , The dotted line is the actual signal of the measuring line S. However, the detected signal waveforms at S-P1 ~ P4 are disagree with from the actual signal. This proves that secondary electrons which are emitted at measuring line S have high sensitivity to electrostatic field which is generated by R.

On the other hand, Fig. 4(c) show the detected signal waveforms at S-P5 ~ P7 which have the shield metal. An aluminium (Al) and a molybdenum silicide ($MoSi_2$) shield line surround the measuring point P5 and P6, respectively. These shield line are grounded level. It should be noted that the detected signal waveforms at S-P5 ~ P7 are reduced the effect of the neighboring pattern signal. Moreover, these data show that $MoSi_2$ shield line has the same shield effect as Al line.

Furthermore, a two dimensional electric field analysis was performed to study the local electric field effect and the shielding effect. Fig. 5 shows a plot of the potential distribution in the cross section through R and S by using two dimensional computer simulation. Fig. 5(a) is no shielding case, and (b) is shielding case. The secondary electrons emitted at the measuring point are detected by photomultiplier tube PMT through a retarding field where R catches the secondary electrons. The retarding field with shield metal is less than that without shield metal by 0.2V. This voltage is relatively large since the maximum of the energy distribution of secondary electrons occurs at a few electronvolts. The electric field potential of various interval case between R and S was compared with shielding metal case, as shown in Fig. 6. It is clear that shielding metal effect is more effective than the other various interval case. The calculated results show reasonably good agreement with the experimental data, as shown in Fig. 4.

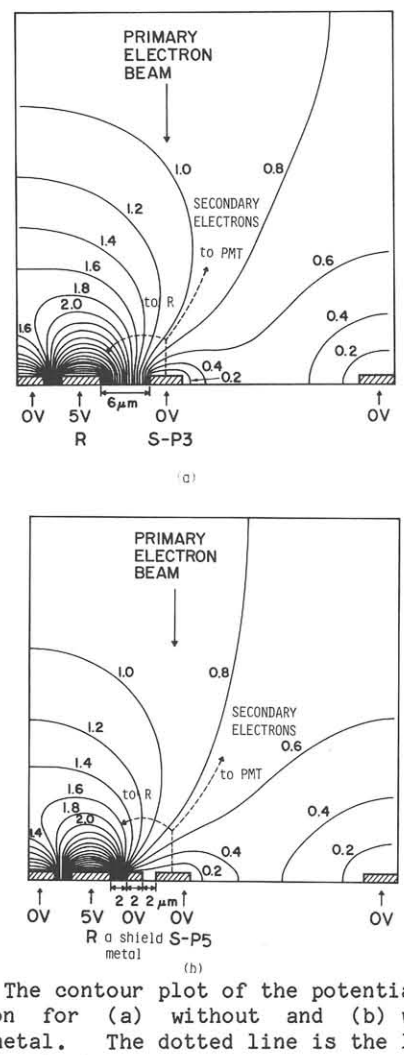


Fig. 5 The contour plot of the potential distribution for (a) without and (b) with the shield metal. The dotted line is the locus of secondary electrons.

3.2 The electron beam effect

The second problem is the electron beam effect on the internal floating node potential of the dynamic RAM. The pulsed beam current of 4nA with 2ns pulse width is selected to reduce this effect. Fig. 7 shows the schematic circuits of memory cells and a sense amplifier and a timing diagram. Fig. 8 shows the measured waveforms of the memory

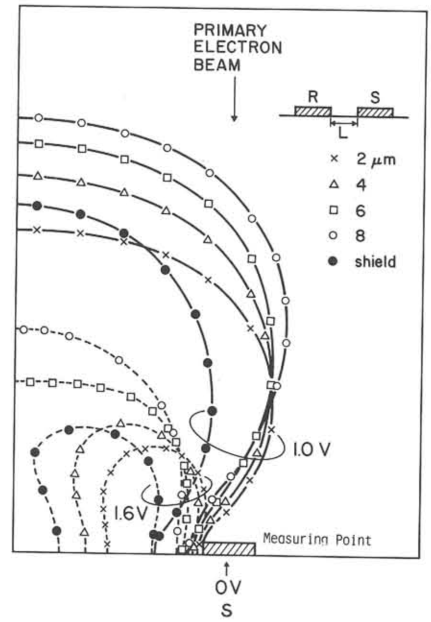


Fig. 6 The contour plot of the electric field potential for several interval and with shield metal.

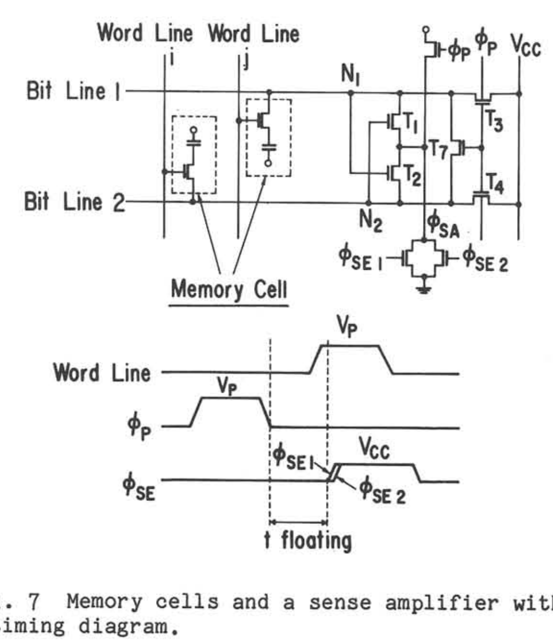
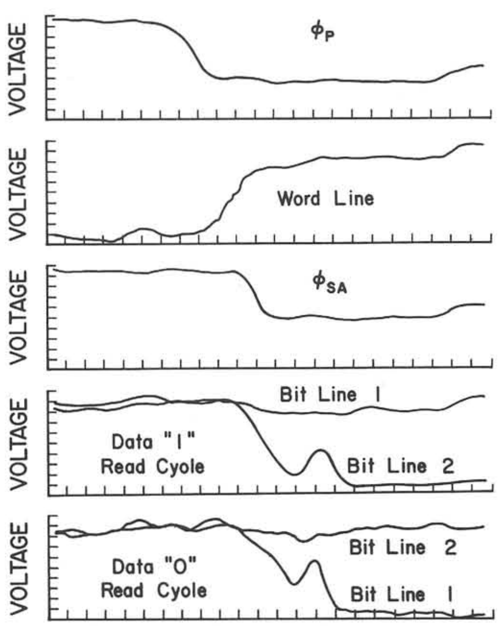


Fig. 7 Memory cells and a sense amplifier with a timing diagram.

array. The capacitance value of the floating bit lines is 400fF, and the voltage effect of the electron beam is less than 0.02mV and negligibly small. As shown in this figure, the bit line signal can be measured correctly by this condition.

Utilizing these measuring techniques with improved accuracy, the clock simulated waveforms.



10(ns/DIV) Y:Arbitrary unit

Fig. 8 Measured waveforms of the memory array signals.

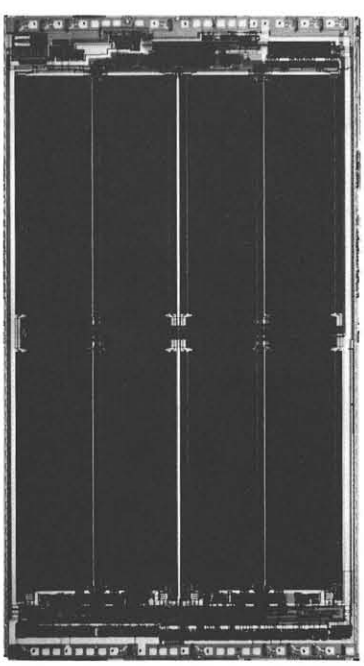
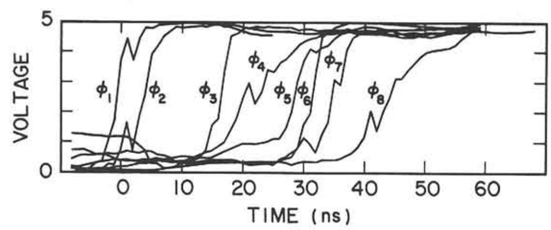
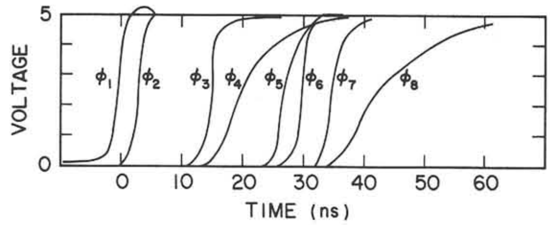


Fig. 9 Microphotograph of the 256k dynamic RAM; chip size is 5.0 x 9.2mm.



(a) WAVEFORMS MEASURED BY ELECTRON BEAM TESTER



(b) SIMULATED WAVEFORMS

Fig. 10 Measured and computer simulated clock sequences.

Fig. 9 and Fig. 10 show the newly developed 256k dynamic RAM and the measured and computer simulated clock sequences, respectively.

4. Conclusion

Electron beam testing techniques for dynamic memory devices have been successfully developed. Good accuracy is obtained by introducing shielding technique and optimized beam condition. The internal timing analysis utilizing this electron beam testing and computer simulation makes it possible to optimize the circuit design of dynamic memory LSI's which contain the complex clock sequences.

Acknowledgements

The authors wish to thank K. Odagawa and Y. Nishi for their continuous encouragement, Y. Uchida and K. Natori for valuable discussions and suggestions, K. Okumura, M. Miyoshi and M. Ishikawa for their advices in the experiments, H. Ishiuchi, Y. Takeuchi and M .Ishikawa and S .Asami for their valuable contributions and support.

References

1) H. Fujioka, K. Nakamae and K. Ura: IEEE J. Solid-State Circuits SC-15 (1980) 177.
2) M. Sato and S. Saito: Paper Tech. Group on SSD, IECE Jpn. SSD82-74 (1982) 31.
3) K. Natori, T. Furuyama, S. Saito, S. Fujii, H. Toda, T. Tanaka and O. Ozawa: ISSCC Digest of Tech. Papers (1983) 232.
4) M. Miyoshi, M. Ishikawa and K. Okumura: Scanning Electron Microscopy (1982) 1567.