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180-Bit Static Shift Register and Driver Using Poly-Silicon MOSFFTs

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Poly-silicon gate self-aligned poly-silicon MOSFETs were fabricated on a transparent glass substrate using a low temperature process (< 520 °C). Inverter propagation delay time and power dissipation are 95 nsec and 0.65 mW at V_{DD} = 30 V. The 180-bit static shift register and driver, using poly-silicon gate self-aligned MOSFETs, was operating at 5 - 100 kHz clock frequency. This 180-bit device has a high enough voltage level to drive the poly-silicon TFTs on LCD panel. This device can drive more than 1600 gate lines on an LCD panel to display TV pictures.

§ 1. Introduction

As the liquid crystal display (LCD) resolution is higher and the dispaly area is larger, the date signal drivers as well as active matrix elements need to be formed on the same substrate using monolithic technology in order to reduce the large number of interconnections between the LCD panel and the external signal drive circuits.

In the past few years, a fully integrated LCD, formed on the crystalline silicon substrate, was reported.[1] However, such an LCD on a glass substrate, having large area and transparent possibilities, has not been reported.

The present work shows fabrication and evaluation for the shift register as an LCD driver, using poly-silicon MOSFETs on the glass substrate. Poly-silicon MOSFETs having electrical properties necessary for use in LCD drive circuits have been reported.[2,3] However, it is necessary to establish the self-aligned MOSFET technology in order to fabricate a large scale shift register on glass substrate.

§ 2. Poly-silicon gate self-aligned MOSFET

In the present work, poly-silicon films are used for gate materials, as well as for MOSFET materials. The poly-silicon films were e-gun evaporated in high vacuum (< 5 x 10^{-7} Torr) on a HOYA NA - 40 glass substrate with a 75 mm diameter.

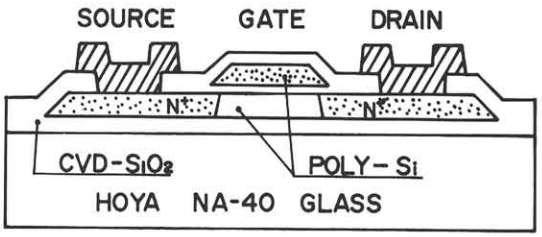


Fig. 1 Cross-sectional view of the poly-silicon gate self-aligned poly-silicon MOSFET

Figure 1 shows a cross-sectional view of the poly-silicon gate self-aligned poly-silicon MOSFET. Substrate temperatures during silicon evaporation were 520 °C for MOSFET materials and 480 °C for gate materials. Films were about 0.4 μm thick. 1500 Å thick CVD - SiO_2 films, deposited at 500 °C, were used for the gate insulator for MOSFETs. Due to higher mobility and lower threshold voltage for N-channel MOSFETs, the source and drain regions were formed by phosphorus ion implantation with 2 x 10^{15} cm^{-2} at 170 keV.

The field effect mobility (μ_{eff}) and the threshold voltage (V_T) for poly-silicon gate self-aligned MOSFETs with 8 μm channel length (L) and 48 μm channel width (W) are 15 cm^2/V·sec and 8 V, respectively. These values are nearly equal to those for the conventional aluminum gate poly-silicon MOSFETs.[2] The exchange of poly-silicon for aluminum in gate material has hardly any effect

on the electrical properties for poly-silicon MOSFETs on glass substrates.

To evaluate the inverter switching speed, the propagation delay time (τ_{pd}) was measured in a ring oscillator. It consists of 21-stage inverters with a 2.0 fan-out. The W/L values for the load and that for the driver for these inverters are 8 μm/8μm and 48μm/8μm, respectively. The 3-stage output buffer amplifier is connected to the ring oscillator in order to observe the oscillation waveforms.

Figure 2 shows the dependence of propagation delay time and power dissipation (P_W) for poly-silicon gate inverters on supply voltage (V_{DD}), and, for reference, shows these for a conventional aluminum gate inverter having 3.5 fan-out and the same W/L values. Although the slopes of the line in τ_{pd} or P_W for self-aligned inverters are almost equal to those for conventional inverters, τ_{pd} and P_W for self-aligned inverters are about half of the values of conventional inverters, because of the smaller fan-out. The 95 nsec propagation delay time is obtained at V_{DD} = 30 V, which shows that the inverter can operate close to 5 MHz.

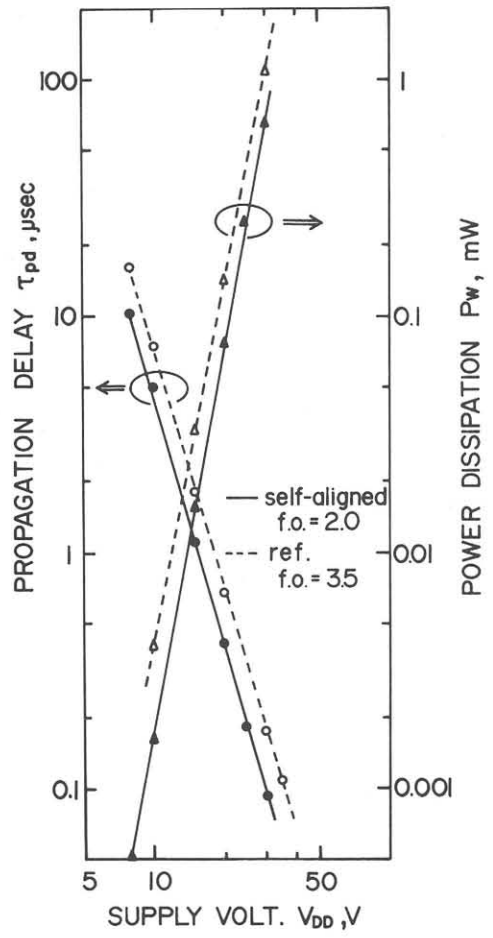


Fig. 2 Propagation delay time and power dissipation vs supply voltage for self-aligned MOSFETs. Dashed lines are Oana's (2) results.

§ 3. 180-bit static shift register and driver

A 180-bit static shift register and driver was designed and fabricated on the basis of the results obtained for poly-silicon gate self-aligned MOSFETs on the glass substrate. This device consists of 180-stage two-phase D-type flip-flops and 180 buffer/drivers. Figure 3 shows the circuit

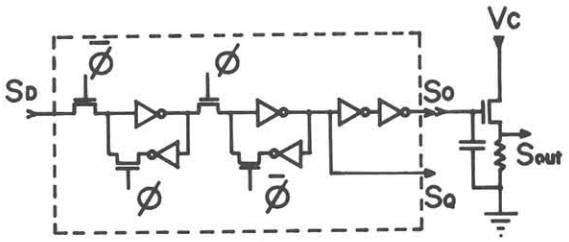


Fig. 3 Circuit diagram for one-bit delay and driver for the 180-bit static shift register

diagram for one-bit delay and the driver for this 180-bit device. The output signal (S_O) for one-bit device is amplified with an external MOSFET amplifier, observed as the output signal waveform (S_{out}) using a synchroscope. This one-bit device can shift the input data signal (S_D) to the output data signal (S_Q) according to the clock (ϕ and $\bar{\phi}$). The W/L values for the load and that for the driver for the flip-flops inverter are 8μm/8μm, respectively.

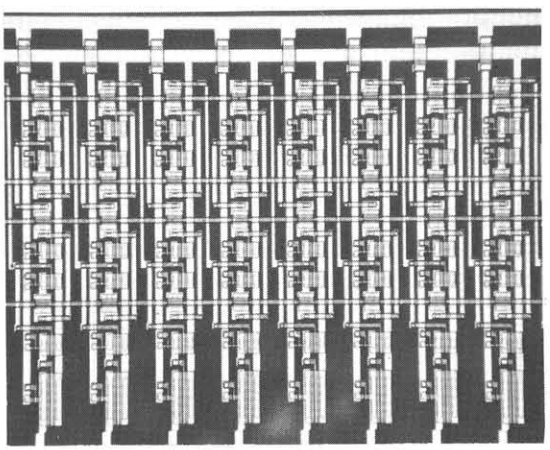


Fig. 4 Microphotograph of a portion of the fabricated 180-bit device.

Figure 4 shows a microphotograph of a portion of the fabricated 180-bit device. There are four clock lines on each bit area. In this process, one key technique is the tapered-etching of poly-silicon films to prevent poly-silicon gate line breaks. The one-bit area is 1400 μm x 200 μm and the 180-bit device area is 1.4 mm x 36.0 mm.

Figure 5 shows the waveforms for the clock (ϕ) and input/output signals (S_D and S_{out}) for the 180-bit device at various clock frequencies (f_c). At the 30th bit of the 180-bit device, the waveforms were observed at 5 kHz, 10 kHz and 100 kHz clock frequencies. These results are shown in Figs. 5(a), 5(b) and 5(c). In these measurements, the clock signal voltage (V_ϕ and $V_{\bar{\phi}}$) and the input data signal voltage (V_{S_D}) have the same values. They are about 5 V lower than the supply voltage value. As the clock frequency increases, higher voltages are applied to the 180-bit device in order to transfer the date signals. The maximum and minimum clock frequency able to transfer data signals are not clear at present, but optimizing the timing between clock and input data signal can transfer the data signal at higher or lower clock frequency.

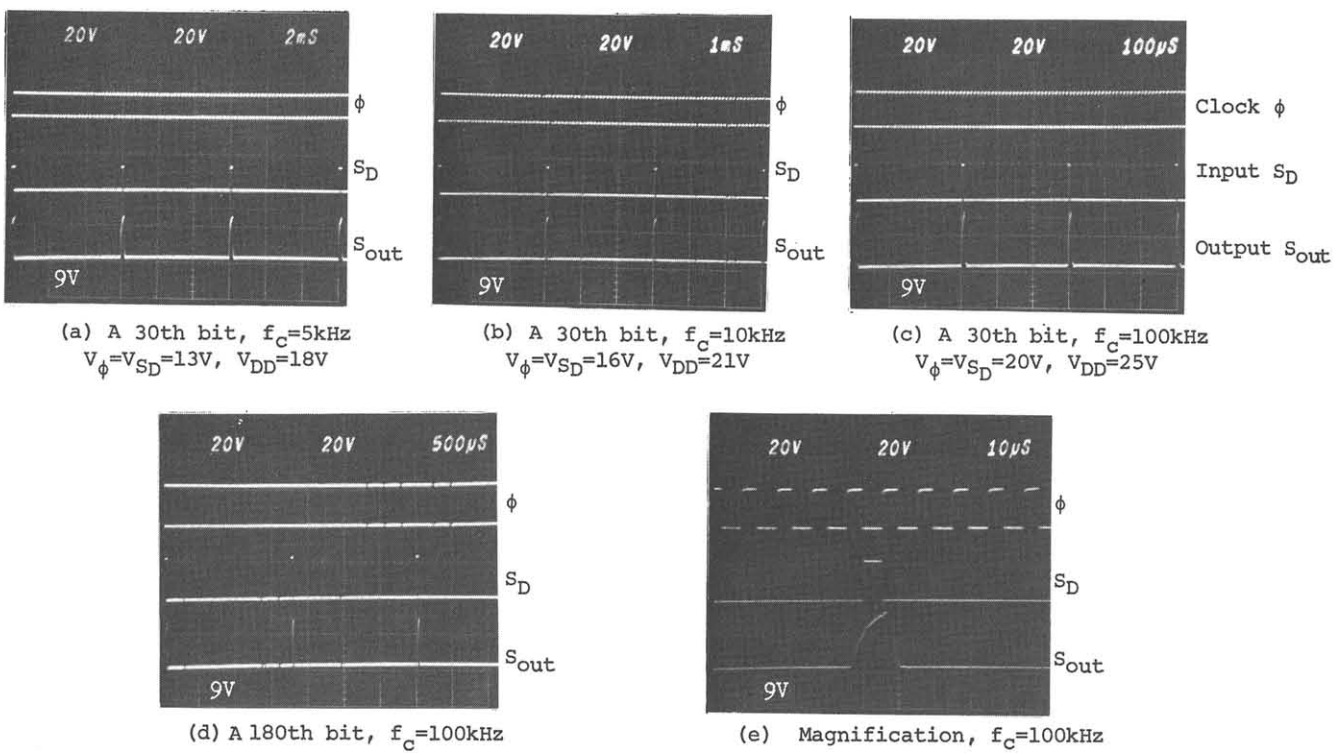
Figure 5(d) shows clock and input/output signal waveforms for the 180-bit device at 100 kHz clock frequency. Output signal waveforms, delayed by 1.8 msec (= 10 μsec x 180 bits), are observed at the input signal position on the time scale.

The signal waveforms magnifying the time scale are shown in Fig. 5(e) at 100 kHz clock frequency. The output signal should rise and then fall as the clock turns on, in theory. However the rise time or fall time for an output signal are delayed about 1 μsec, compared with clock ϕ. The low- and high-voltage levels for the output signal (S_{out}) are 2 V and 17 V, respectively, at V_{DD} = 25 V. These values are sufficient for controlling poly-silicon MOSFET gate voltages.

§ 4. Conclusion

Poly-silicon gate self-aligned MOSFETs were fabricated on glass substrate. N-channel MOSFETs have more than 10 $cm^2/V \cdot sec$ field effect mobility and 8 V threshold voltage. Propagation delay time and power dissipation for the self-aligned inverter are 95 nsec and 0.65 mW at V_{DD} = 30 V.

A 180-bit static shift register and driver using poly-silicon gate self-aligned MOSFETs was



(a) A 30th bit, f_c=5kHz
V_ϕ=V_{S_D}=13V, V_{DD}=18V

(b) A 30th bit, f_c=10kHz
V_ϕ=V_{S_D}=16V, V_{DD}=21V

(c) A 30th bit, f_c=100kHz
V_ϕ=V_{S_D}=20V, V_{DD}=25V

(d) A 180th bit, f_c=100kHz

(e) Magnification, f_c=100kHz

Fig. 5 Clock (ϕ) and input/output signal (S_D snd S_{out}) waveforms for fabricated 180-bit device

fabricated on the glass substrate. This 180-bit device was operating at 5 - 100 kHz clock frequencies and the data signal transfer was observed over 180 buffer/drivers. The difference between the high- and low-voltage level for the output signal is more than 15 V at V_{DD} = 25 V. These values are enough to control the gate voltage for poly-silicon MOSFETs on an LCD panels. The 180-bit device can drive more than 1600 gate lines in an LCD panel with a frame rate of 60 frames/sec. However, the design rule for the shift register/driver and the timing diagram must be optimized to get the best circuit performance.

Acknowlegements

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