

## Invited

## GaAs Digital Integrated Circuits

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This paper describes an overview of fabrication, performance, and bit-yield of the 1Kb static RAM fabricated using SAINT (Self-Aligned ion-Implantation for  $N^+$ -layer Technology) as a GaAs LSI feasibility study. The highest speed operation of 1.5 ns X-address access time with a power dissipation of 369 mW was obtained. The typical threshold voltage standard deviation of a processed 2-inch LEC wafer was 50 to 60 mV. The standard deviation per chip was reduced to be 27 mV. The deviation was analyzed and found to be mainly due to dislocation effect and dispersion of gate length.

## 1. Introduction

Recent advances in the GaAs IC complexity and performance have proved the practical feasibility for high speed digital circuits. The state-of-the-art performances of GaAs LSIs of 1.5 ns access time 1 Kb static RAM<sup>1)</sup> and 10.5 ns multiply time 16 x 16 bit parallel multiplier<sup>2)</sup> have demonstrated several times faster operation than those of the equivalent circuits in silicon.

Accordingly, GaAs processing technology is now facing to establish a high yield manufacturing technology. It is the purpose of this paper to evaluate the present device and fabrication technology aiming at LSI, which we have been developing, as an example, and to clear up the cause of nonuniformity of the FET electrical characteristics.

## 2. Fabrication

To meet the requirement of threshold voltage controllability and series resistance reduction for MESFETs applicable to GaAs LSIs, several approaches have been extensively investigated<sup>3~7)</sup>. We have developed a new fabrication technology named SAINT; Self-Aligned ion-Implantation for  $N^+$ -layer Technology<sup>4)</sup>, by which  $n^+$ -layer can be embedded into parasitic resistance regions at an arbitrarily controlled distance from the gate by under-cutting the

multilayer resist as a stopping mask for the  $n^+$ -implantation.

The cross section of thus fabricated SAINT MESFET IC is depicted in Fig 1.

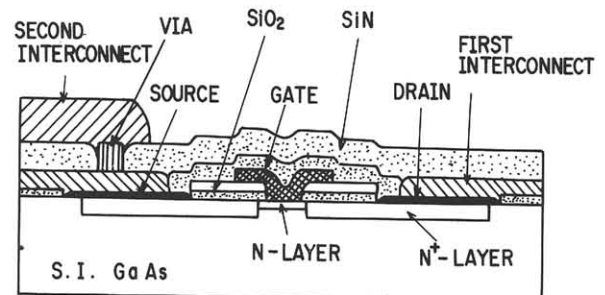
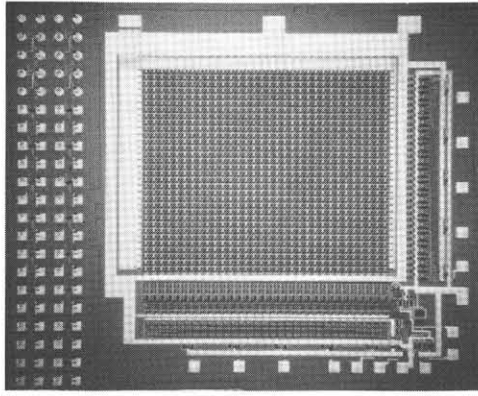


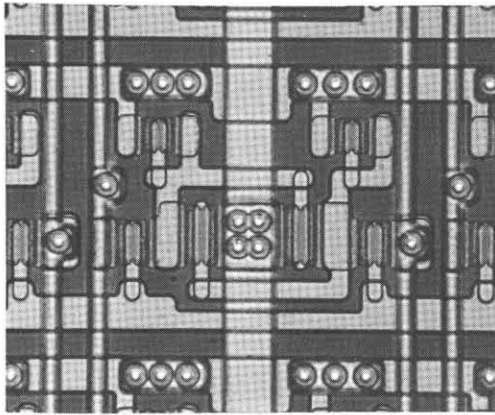
Fig. 1 Cross section of SAINT MESFET IC.

The advantages of SAINT are summarized as follows. (1) Throughout the process, FET surface is covered by a p-CVD passivation SiN film which is also served as a cap material for the post-implantation annealing. (2) Schottky gate barriers are formed after the annealing. They are greatly contributed to make the FET characteristics stable and reproducible.

Figure 2 shows a 1 Kb static RAM chip microphotograph and Table 1 gives characteristics summarized. This RAM is an advanced version of the previously reported one<sup>8)</sup>, where a bit-line pull-up circuit was added for high speed reading and a gate direction was arranged in one direction for avoiding the FET



(a)



(b)

Fig. 2 Microphotographs of a GaAs 1 Kb static RAM accompanied by monitoring FETs (a) and a memory cell (b). The RAM chip size is 3.42 mm x 3.40 mm and memory cell 69  $\mu\text{m}$  x 57  $\mu\text{m}$ .

Table 1 GaAs 1 kb static RAM characteristics

Device	SAINT MESFET
Gate length	1 $\mu\text{m}$
Line/space	3 $\mu\text{m}$ / 3 $\mu\text{m}$
Through hole	2 $\mu\text{m}$ / 2 $\mu\text{m}$
Organization	1024 words x 1 bit
Cell size	69 $\mu\text{m}$ x 57 $\mu\text{m}$
Chip size	3.42mm x 3.40mm
Element	7148 FETs ( E; 4875, D; 2273 )
Configuration	E/D DCFL
Threshold voltage	E; 52mV, D; -507mV
Standard deviation	E; 66mV, D; 89mV
Access time	1.5ns
Power dissipation	369mW
Supply voltage	V <sub>c</sub> =1.6V, V <sub>p</sub> =0.8V

drain current difference between X and Y directions.

As semi-insulating substrates for direct Si-ion implantation for E, D and n<sup>+</sup>-layers, LEC grown 2-inch GaAs crystals doped with Cr ranged

from 0.1 to 0.3 wt.ppm were used. Averaged etch pit density was around  $3 \times 10^4 / \text{cm}^2$ .

### 3. Performances

The processed wafers were function-tested by on-wafer probing and X-address access time was measured for the selected chips after packaging.

The minimum access time of 1.5 ns with a power dissipation of 369 mW was obtained at a cell and a peripheral circuit supply voltages of 1.6 and 0.8 V, respectively. The averaged access time was about 2 ns.

### 4. Yield and Dispersion

The 0-1-0 write-function test was performed for the 32 bit cells on the diagonal line in the 1024 bit memory area. In Fig. 3, the pass bit yield was shown against the threshold voltage standard deviation measured for 20 monitoring enhancement-mode FETs with gate length of 1  $\mu\text{m}$  and width of 9  $\mu\text{m}$  accompanied with each 1 Kb RAM chip. The full bit operation out of 32 bits was obtained for the standard deviation of 27 mV, whose chip showed 98 percent bit-yield in total, namely 1001 pass bits out of 1024 bits. The chip exhibited 1.6 ns access time at 286 mW power consumption.

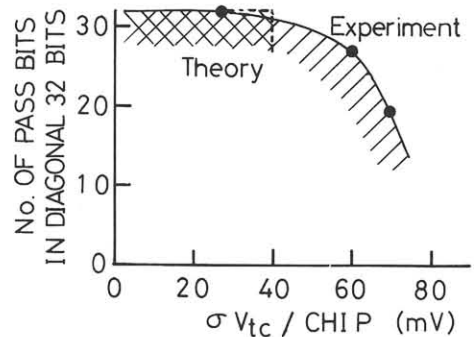


Fig. 3 Bit-yield out of 32 bit cells on the diagonal line in 1 Kb memory area versus FET threshold voltage standard deviation per chip measured by the monitoring enhancement-mode FETs.

According to the statistical analysis for 1 Kb static RAM using ASTAP program, the allowable threshold voltage standard deviation for retaining normal operation was estimated to be

about 40 mV. The experimental measurement resulted in somewhat lower value.

The threshold voltage for the monitoring enhancement-mode FETs on a typical 2-inch processed wafer was plotted against gate length and short channel factor  $N_G$ , which is introduced as  $I_{ds} \propto \exp(qV_{gs}/N_G kT)$  in the subthreshold region<sup>9)</sup>, in Fig. 4. Gate length dispersion from 1.25 to 0.85  $\mu\text{m}$  can be found, which was inevitable with the conventional contact lithography utilized. The dispersion arised from the  $n^+$ -patterning and did not from the side etching of tri-level resist in SAINT. The threshold voltage scattering of about 200 mV from minimum to maximum found at constant gate length, we believe, comes from the substrate crystal inhomogeneity. Fig. 4 gives threshold voltage standard deviation of 56 mV over 2-inch wefer, in which those originated from gate length dispersion and crystal inhomogeneity are 44 mV and 35 mV, respectively.

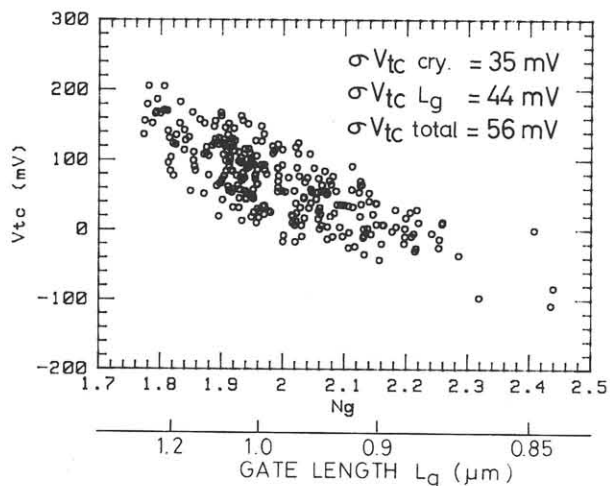


Fig. 4 FET threshold voltage versus gate length of monitoring FETs on a 2-inch processed LEC wafer.

### 5. Discussions and Conclusion

As far, two major causes for the threshold voltage dispersion has been made evident. The gate length dispersion will be halved, providing more refined lithography such as reduction projection alignment and/or EB direct writing, as well as improving device structure to reduce

short channel effect. In other experiment, we applied EB direct writing to gate patterning and were able to obtain precisely controlled 0.3  $\mu\text{m}$  gate length<sup>10)</sup>.

As for crystal inhomogeneity, a clear and very important correlation of FET threshold voltage versus a distance between FET and dislocation pit in low Cr doped LEC crystal has been revealed more recently, although the FET had the conventional structure for evaluation purpose<sup>11)</sup> (Fig. 5). The existance of the well

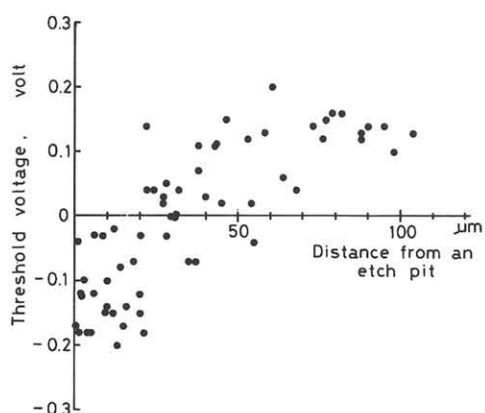


Fig. 5 FET threshold voltage versus distance between the FET and a nearest dislocation pit for a LEC crystal with etch pit density around  $3 \times 10^4 / \text{cm}^2$  (11).

known 20 to 30  $\mu\text{m}$  radius denuded zone around dislocation affects FET threshold voltage, and it was found the maximum difference in threshold voltage was about 300 mV between inside and outside the denuded zone around dislocation. Mechanism of the denuded zone should be analysed and some effective technologies of homogenizing the crystals should be developed. Otherwise, dislocation-free crystals are strongly demanded.

When the problems described above are solved, the yield of GaAs LSIs will surely be improved up to be applicable to factory production.

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