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A 4×4 Bit Parallel Multiplier with GaAs JFET DCFL

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GaAs ICs with normally-off p-n junction FETs satisfying high-speed and low-power requirement have shown high yield capability. The threshold voltage of the JFET can be monitored on chip and adjusted by additional drive-in diffusion.
A 4x4 bit parallel multiplier with JFET DCFL has been successfully fabricated and has exhibited good performance with high fabrication yield. The multiplier chip contained 156 gates and measured 2.6x2.3 mm^2 including bonding pads. The functionality testing was carried out for all input data combinations and assured all gates were working. High-speed performance was evaluated by the time required for the signal to propagate through the critical path loop. The corresponding path delay of 15 t_{pd} was 3.5 nsec. The power dissipation ranged from 20 to 70 mW at a supply voltage of from 0.8 to 1.3V.

I. Introduction

Recent works on GaAs logic circuits using normally-off MESFETs have demonstrated high-speed and low-power MSI and LSI applications.[1-4] The MESFET DCFL gate is a possible approach for GaAs MSI/LSI but has the difficulty in controlling the threshold voltage of the FETs. Our JFET technology can precisely control the threshold voltage for any carrier concentration profile in the n-channel layer by manipulating the depth of the p-n junction which is monitored on-chip and adjusted by additional drive-in diffusion.[5] This technique makes it possible to obtain JFETs with a required threshold voltage even if the channel layer profile deviates from the desired one, as is often the case with the present day GaAs substrate. The JFET has other advantages of higher logic swing and higher noise margin due to higher built-in voltage of the p-n junction. Therefore, ICs with JFET gates were expected to have high yield capability.

The 4x4 bit multiplier is a test vehicle to evaluate the JFET MSI/LSI. The first GaAs JFET MSI has demonstrated good performance with high fabrication yield.

This paper describes design, fabrication and performance of the GaAs 4x4 bit multiplier with the p-n junction FET.

II. Multiplier Circuit Design

The basic gate utilized in the design of the multiplier is a DCFL NOR gate. The DCFL gate is composed of the normally-off JFET and the resistive load, i.e., E/R DCFL. The gate propagation delays for the E/R and the E/D were measured for a range of dissipation power and are compared in Fig. 1. The significant differences in performance between E/R and E/D have not been observed as seen in the figure. E/R DCFL was employed in the multiplier design because of its higher homogeneity and run-to-run reproducibility.

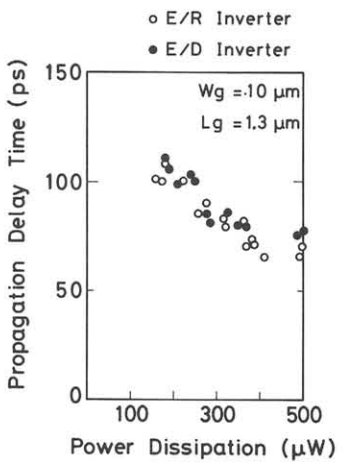

Fig. 1. Propagation delays for E/R and E/D

Typical current-voltage characteristics of the JFET with the threshold voltage of 0.2 V is shown in Fig. 2. It has a gate width of 10 μm and a length of 1.5 μm. Since large forward gate

bias of 1.2 V can be applied to the JFET without appreciable gate current, it has high saturation current and high transconductance.

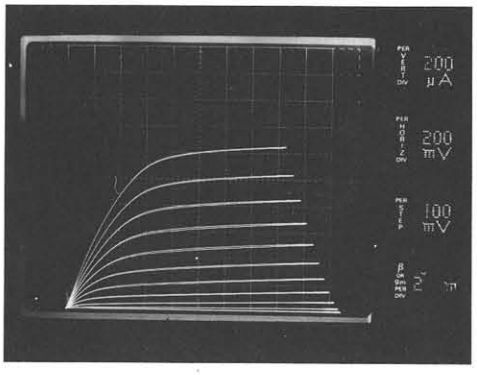

Fig. 2. Typical current-voltage characteristics of the 10 μm wide JFET. V_{th}=0.2 V.

Although low resistive loads ranging from 1.5 to 2.5 kohm had been used for the E/R gate so far to optimize the performance, higher resistive loads were selected in the design of the 4x4 bit multiplier to make the E/R gate less sensitive to the fluctuation of JFET performance. Experimental results and simulations have indicated that 3 kohm load, for example, improves the logic swing by 120 mV, the noise margin by 70 mV, and the power dissipation by 50 μW sacrificing the propagation delay by 20 psec compared to 2 kohm load.

The parallel array architecture with the carry save was employed for the design of the 4x4 bit multiplier. A block diagram of the 4x4 bit multiplier is shown in Fig. 3. It comprises 4 half adders (HA), 8 full adders (FA) and 16 NOR gates. In addition to the array, the self-test feedback path was included as shown in the figure. The logic diagram of a full adder cell is shown in Fig. 4. The 4x4 multiplier chip included 156 gates and measured 2.3x2.6 mm^2 including bonding pads. The chip covers large area in order to evaluate the potential for the LSI application. A micrograph of the multiplier chip is shown in Fig. 5.

III. Fabrication

Fabrication features for planar GaAs JFET ICs are the following: 1) selective ion implantation of Si directly into the semi-insulating substrate; 2) capless anneal; and 3) selective Zn diffusion, whose depth is adjusted to the desired

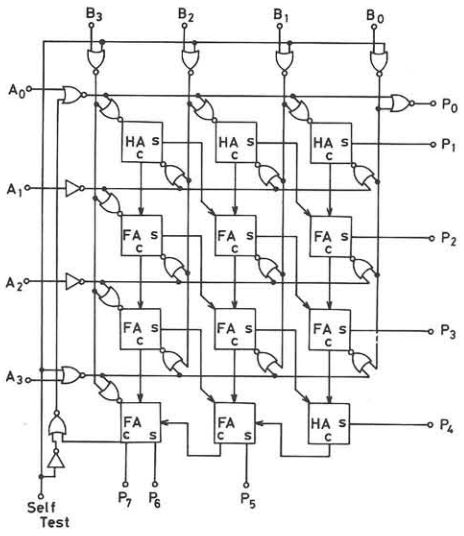

Fig. 3. Block diagram of the 4x4 bit parallel multiplier. The self-test feedback path is shown in the figure.

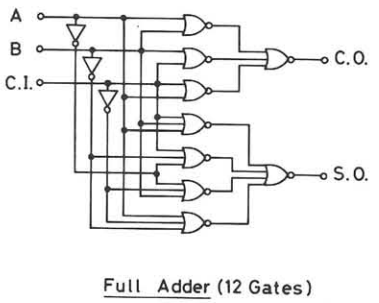

Fig. 4. Logic diagram of a full adder cell.

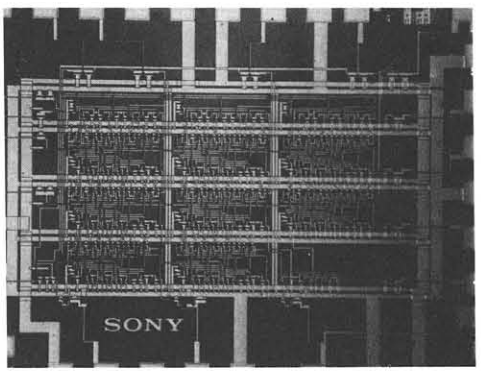

Fig. 5. Microphotograph of the 4x4 multiplier chip. The chip covers 2.3x2.6 mm including bonding pads.

threshold voltage.

The n-type areas were formed by selective Si implantation directly into the semi-insulating GaAs substrate. No significant differences in performance or fabrication yield have been observed between HB and LEC, or Cr-doped and undoped substrates so far as substrates were qualified. Typical implantation parameters for the E-JFET channel and the n^+ contact region were 130 keV, $4x10^{12}$ cm^{-2} and 200 keV, $1x10^{13}$ cm^{-2}. After ion implantation, the wafers were annealed at 850 C for 15 min under arsine partial pressure of 3.0 torr without any dielectric film.[6] The average sheet resistivities were 550 and 160 ohms/sq for the E-channel and the n^+ region.

P-n junctions for the gates were formed by selective Zn diffusion using an open tube system. A 100-nm-thick silicon nitride film deposited by the plasma enhanced CVD technique, was used as a diffusion mask. Anomalous lateral diffusion was not observed and the lateral diffusion was about 80% of in-depth diffusion. The diffusion constant of Zn at 600 C was estimated to be $7x10^{-14}$ cm^2/s in our diffusion system. The diffusion time was about 30 min for the E-JFET whose active layer was made by Si implantation of $4x10^{12}$ cm^{-2} at 130 keV. The surface doping density of the p region exceeded $5x10^{19}$ cm^{-3}, which was high enough to use direct metal contact probe to the p diffused region for C-V measurement. Therefore, the pinch-off voltage of the JFET can be monitored on the chip by C-V method as schematically shown in Fig. 6. The pinch-off voltage was adjusted by additional drive-in diffusion if necessary.

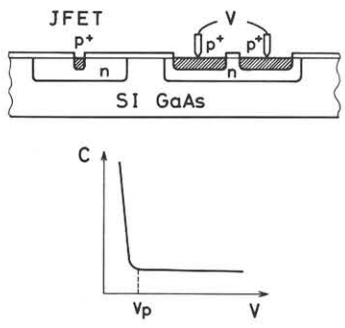

Fig. 6. Schematic diagram of the pinch-off voltage monitor for the JFET. C-V curve for p-n-p is shown in the figure.

The ohmic contact metals of Ni/Au-Ge/Au for n-type and Ti/Pt/Au for p-type were formed by lift-off method assisted by SiO_2 spacer. After the surface was covered with a 300 nm thick SiN film, Ti/Au interconnection was defined using ion milling.

The threshold voltage uniformity and reproducibility of the E-JFET for 8 slices used to fabricate the multiplier was characterized by the average value of 0.220 V with a standard deviation of 109 mV.

IV. Multiplier Evaluation

Figure 7 shows the functionality testing for the full adder. Two traces correspond to the sum output (upper) and carry output (lower), where A input, B input and carry input are applied as following combinations of 001, 100, 010, 110, 101, 011 and 111. The functionality testing for

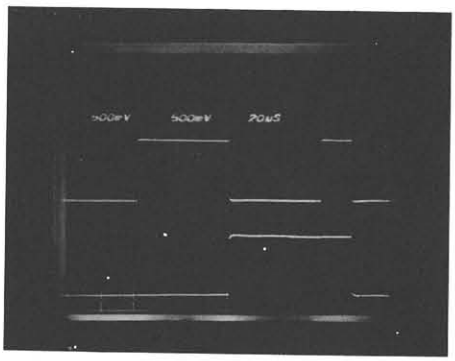

Fig. 7. Functionality testing for the full adder. V_{dd}=1.0 V, I_{dd}=3.6 mA.

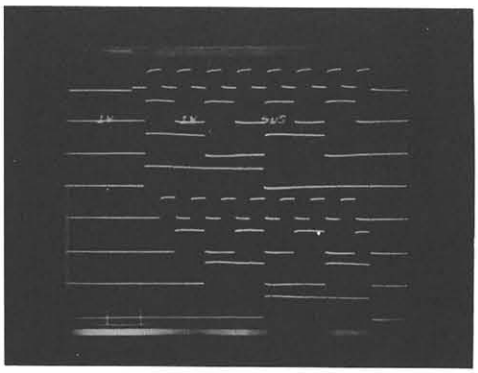

Fig. 8. Operating waveform of 8 product bits of the multiplier at a supply voltage of 1 V and I_{dd}=36 mA. The input codes are 1111x $B_3B_2B_1B_0$, where B_3-B_0 change 16 input data combinations.

the 4x4 bit multiplier was done for all input data combinations of 2^8 (256) by applying square-wave inputs and assured all gates were working. Fig. 8 demonstrates the operating waveform of 8 product bits of the multiplier at a supply voltage of 1 V. The input codes are 1111x$B_3B_2B_1B_0$, where the combinations of $B_3B_2B_1B_0$ change as 0000, 0001, 0010, 0011, 0100, 0101, 0110, 0111, 1000, 1001, 1010, 1011, 1100, 1101, 1110 and 1111.

High-speed performance was evaluated by the time required for the signal to propagate through the loop from the most significant product bit (P_7) to the least significant input (A_0) as shown in Fig. 3. In the self-test mode, ringing oscillation is observed and its frequency is determined from the propagation delay through the loop (A_0 to P_7: 15 t_{pd}). Fig. 9 shows the output waveform of the multiplier operating in the ring oscillator mode with input $B_3B_2B_1B_0$=1111 and $A_3A_2A_1A_0$=100S, where S=$\overline{P_7}$. The corresponding multiplication time would be 3.5 nsec. The main E/R gates of this multiplier comprised 2.6 kohm and the 10 μm wide JFET. The power dissipation ranged from 20 to 70 mW at a supply voltage of from 0.8 to 1.3 V. The multiplication time and the power dissipation depended on load resistance. Multiplication time ranging from 4 to 5 nsec was measured when E/R consisted of 3 kohm load and 10 μm JFET. The power dissipation as low as 7.2 mW was achieved at a supply voltage of 0.6 V with a load of 4.5 kohm. The multiplication time was 7.5 nsec. The multiplier with a 3.5 kohm load yielded a multiplication time of 5.8 nsec with a power dissipation of 13 mW at a supply voltage of 0.66 V.

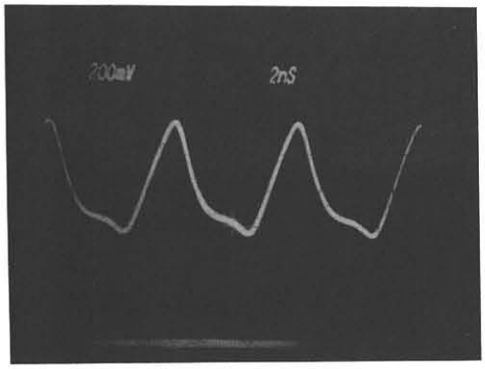

Fig. 9. Output waveform of the 4x4 multiplier when operated in the self-oscillation mode. The corresponding multiplication time is 3.5 nsec. V_{dd}=1.3 V, I_{dd}=54 mA.

Since the threshold voltage of the JFET is adjustable in process and the higher resistive loads were selected for wider allowance of design, more than 50 percent of the multiplier in every slice could be evaluated for self-oscillation operation, and half of them could pass the complete functional testing on average. The circuit yield was limited mainly by the defects generated in the lithography process.

V. Summary

A 4x4 bit parallel multiplier has been successfully fabricated using JFET DCFL gates. A minimum multiplication time of 3.5 nsec was obtained with the power dissipation of 70 mW. A typical multiplication time was 4 to 5 nsec when a 3 kohm load and a 10 μm wide JFET were used for the E/R gates. The power dissipation of 7.2 mW with the multiplication time of 7.5 nsec was achieved with a load of 4.5 kohm. The multipliers in every slice have operated in the self-oscillation mode and half of them have shown full operation.

The first GaAs JFET MSI demonstrates good performance with high fabrication yield and indicates that the JFET DCFL is one of the promising candidates for MSI/LSI application.

Acknowledgements

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