Extended Abstracts of the 15th Conference on Solid State Devices and Materials, Tokyo, 1983, pp. 69-72

Sidewall-Assisted Closely Spaced Electrode Technology for High Speed GaAs LSIs

Asamitsu Higashisaka, Masaoki Ishikawa, Fumiaki Katano, Shuji Asai,
Takashi Furutsuka and Yoichiro Takayama

Microelectronics Research Laboratories, NEC Corporation
1-1, Miyazaki, Yonchome, Miyamae-ku, Kawasaki, Japan

A novel GaAs processing technology has been developed, giving a high GaAs MESFET transconductance (g_m) with a stable fabrication process. Sidewall SiO_2 formed on the side of the gate electrode was employed to separate the electrodes. The developed GaAs MESFET exhibited a much smaller short channel effect than ones with n^+ source and drain regions, and gave a high g_m of 210 mS/mm for the device with the threshold voltage of -0.2 V.

§1. Introduction

To realize high speed GaAs LSIs, a device technology which gives a high GaAs FET transconductance (g_m) with a stable fabrication process is indispensable. Many self-alignment device technologies, such as the SAINT[1,2], the W·Si gate technology[3,4], and the closely spaced electrode technology[5], have hitherto been developed to realize a high g_m GaAs MESFET with reduced source and drain parasitic series resistances.

However, the technologies, which involve n^+ ion-implantation for the source and drain regions, exhibited a short channel effect[2,4], where the threshold voltage (V_T) and g_m of GaAs MESFET shifted anomalously due to the carrier concentration increase caused by the lateral spreading of the implanted ions, and due to the leakage current through n^+ - i - n^+ system. On the other hand, the closely spaced clectrode technology could not realize a satisfactory reduction in the parasitic series resistances, becaue the poor controllability of Al-undercutting prevented a further reduction in the electrode spacings than 0.4μm in a practical level.

The purpose of this paper is to present a new device technology which gives a skillful solution to the above mentioned problems. The new technology is an advanced closely spaced electrode technology, where the gate and source, gate and drain are separated with thin dielectric films formed on both sides of the gate electrode. The fabrication process and the dc characteristics of the new GaAs MESFET are described in Sections 2 and 3, respectively.

§2. GaAs MESFET fabrication procedure

Figure 1 shows a schematic diagram for the GaAs MESFET fabrication process by a sidewall-assisted closely spaced electrode technology. First, a 4000A to 5000A-thick Al gate electrode was formed on the active layer

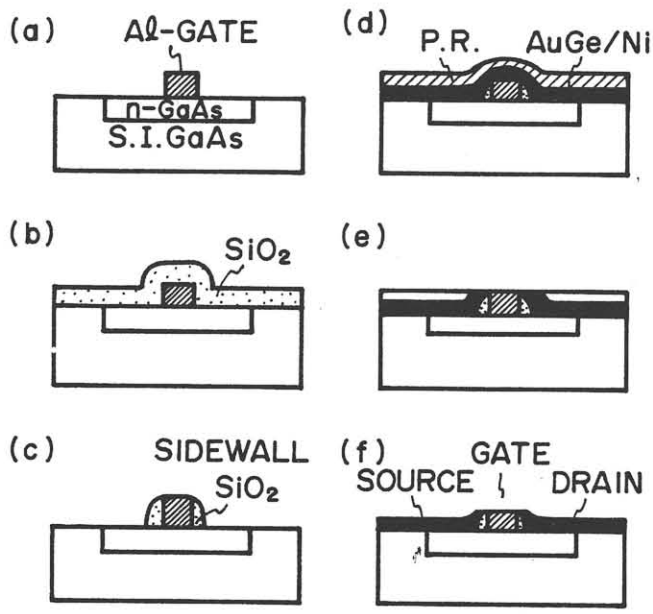

Fig. 1 Process sequence showing cross-section: (a) Gate formation, (b) SiO_2 deposition, (c) Sidewall formation, (d) Ohmic metal evaporation, (e), (f) Selective removal of the ohmic metal from the top of the gate electrode.

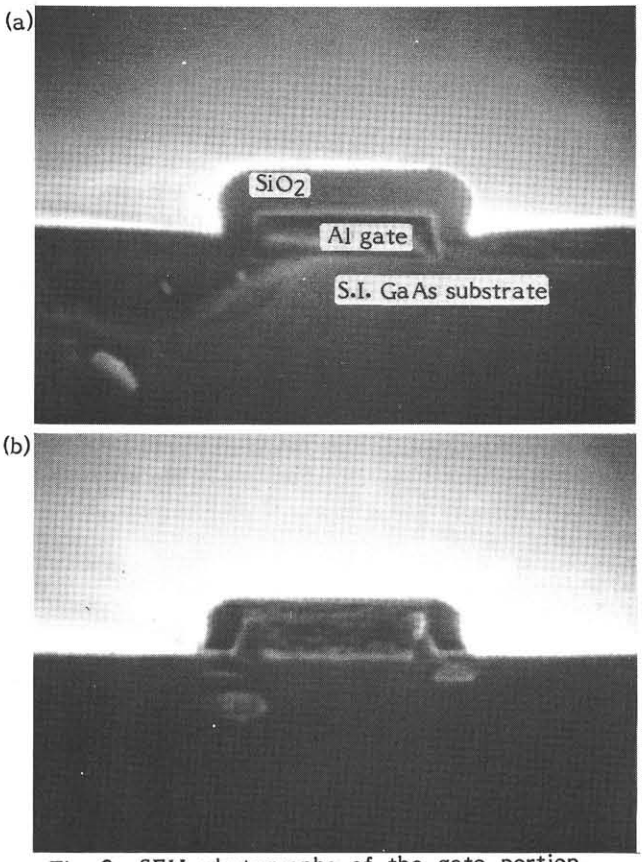

Fig. 2 SEM photographs of the gate portion. (a) Just after SiO_2 was deposited, and (b) Aafter sidewall formation.

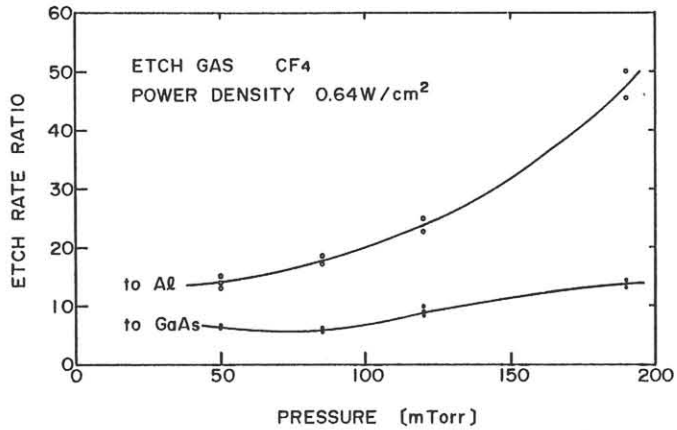

Fig. 3 Dependence of the etching rate ratios of SiO_2 /GaAs, SiO_2/Al on gas pressure.

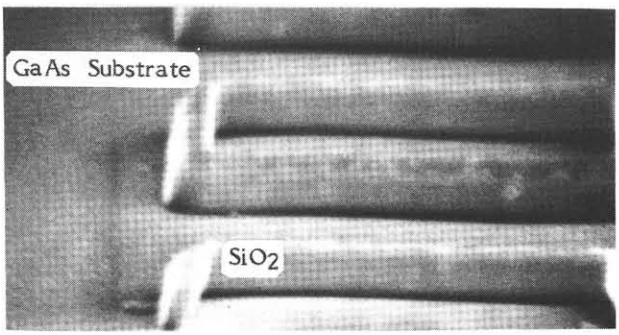

Fig. 4 SiO_2-wall after Al gate is removed.

prepared by the selective implantation of Si^+ into the S.I. GaAs substrate.

Acceleration energy and the dose are 50KeV and 1.8 - $2.8 \times 10^{12} cm^{-2}$, respectively. The steepness of the cross sectional structure of the gate electrode, which is important to achieve a reproducible fabrication of the sidewall, was realized by a relatively large amount of Al undercutting (1 to 1.5μm).

Second, a 2000 to 6000 A-thick SiO_2 film was deposited by a chemical vapor deposition (CVD). A cross-sectional SEM view at this step is shown in Fig. 2(a), where the thicknesses of Al gate and SiO_2 film are about 5000 A and 3500 A, respectively. It is seen from Fig. 2(a) that SiO_2 is well deposited on both sides of the gate electrode with almost the same thickness as on the GaAs substrate field.

Third step is a sidewall formation. A novel technique employing vertical (anisotropic) dry-etching was developed to fabricate the sidewall SiO_2[6]. Both anisotropic and selective etching were achieved by reactive ion etching with CF_4 gas. Figure 3 shows the dependence of the etching selectivity (etching rate ratio) of SiO_2/GaAs, SiO_2/Al on gas pressure. Selectivity increased with increasing gas pressure. For device fabrication, the gas pressure was controlled to 200 mTorr, giving a high (13/1) SiO_2 to GaAs etching rate ratio. RF power, which was found not to influence the anisotropic property so much, was set as low as $0.64 W/cm^2$. Low RF power, as well as the high selectivity, made it possible to fabricate sidewall SiO_2 without damaging the GaAs surface. This is important in obtaining a low ohmic contact resistance and, therefore, a low parasitic series resistances. Figure 2(b) shows an SEM micrograph of the the gate portion after the sidewall oxide formation. The thickness of the sidewall, which determines the spacings between gate and source, and gate and drain, is almost the same (3000 A) as that for deposited SiO_2. This comes from both the anisotropic property of the SiO_2 etching and the steep profile of the Al gate crossectional structure. The sidewall SiO_2 adhered tightly to the GaAs substrate and, as shown in Fig. 4, was not destroyed even after the Al gate is removed.

Fourth step is ohmic metal evaporation. AuGe/Ni film was selectively evaporated on the gate, source and drain region by using a usual photoresist lift off technique.

Fifth step is a selective removal of the unnessessary ohmic metal. To separate the gate electrode from the

source and drain electrodes, the ohmic metal on the top of the gate has to be removed. A unique technology was developed to accomplish this objective, which utilizes the phenomenon wherein the spin-spread photoresist is thinner at the top of the gate than at the bottom field. Figure 5 shows the dependence of the ratio of the resist thickness on the gate to that in the bottom, on the cross sectional profile of the gate electrode. The ratio decreased with increasing the aspect ratio of the gate electrode. In the actual device, where thickness and the length of the gate are 5000 A and 1.2μm, respectively, the thickness ratio is less than 0.6. Anisotropic dry etching with CF_4 is again employed to etch down the photoresist to reveal the ohmic metal on the top of the gate. Ar ion-milling is followed to remove the revealed, unnecessary ohmic metal. GaAs MESFET fabrication is completed by alloying the ohmic metal at 420 °C for 30 secconds.

Figure 6 is an SEM photograph showing an oblique view of a fabricated GaAs MESFET. It is seen that the isolation between the gate and source, and the gate and drain are furnished by dielectric films formed on both sides of the gate electrode. Spacings between these electrodes are not determined by Al-undercutting for the conventional closely spaced electrode structure[5], but by the thickness of the sidewall SiO_2.

§3. Device characteristics

I-V characteristics for the devices fabricated using the technique discussed were measured. Figures 7 (a) and (b) show the typical I_d - V_d and I_{gs} - V_{gs} characteristics observed on a curve tracer, respectively. GaAs MESFET gate width, gate length and sidewall thickness are 8μm,

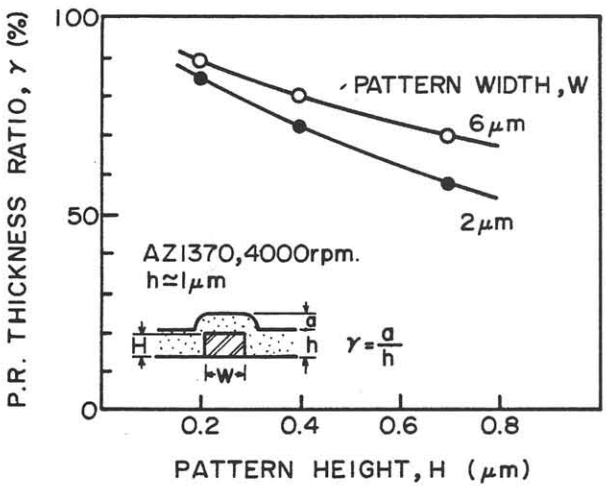

Fig. 5 Dependence of the ratio of the photoresist thickness on the gate to that in the bottom on the cross-sectional porofile of the gate electrode.

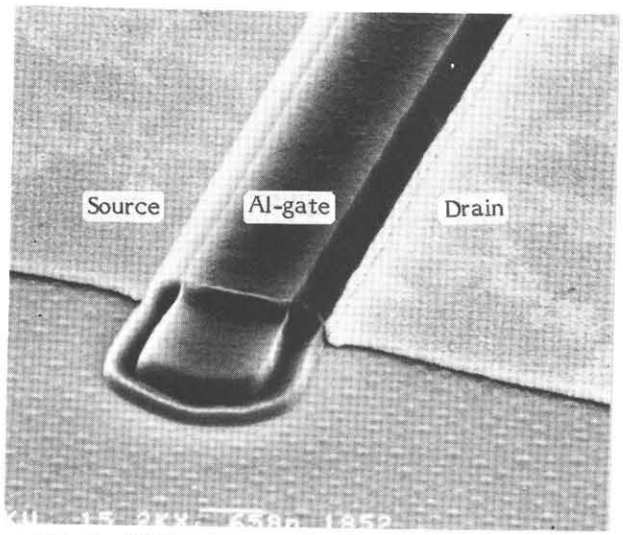

Fig. 6 SEM photograph showing an oblique view of a fabricated GaAs MESFET. Sidewall SiO_2 thickness is, in this care, 0.4μm.

1.2μm and 0.2μm, respectively. The maximum g_m for V_{gs} of 0.6V was 1.7mS (210mS/mm) for the device with V_T of -0.2V. This value is about 1.5 times higher than that of the conventional closely spaced electrode FETs with the spacing of 0.4μm, and is mostly comparable with that of the devices with n^+ source and drain regions. In spite of the narrow spacing between gate and source, the gate breakdown voltage is large (8V) enough for stable and reliable operation of the GaAs MESFET.

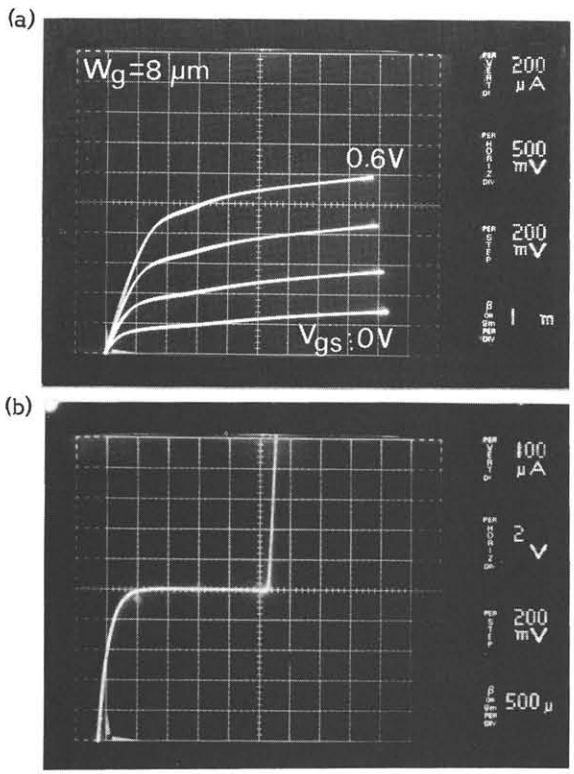

Fig. 7 (a) I_d - V_d characteristics, (b) Igs-Vgs characteristics of the developed device with 0.2um-thick sidewalls.

The most important feature of the new device over the devices with n^+ implanted source and drain regions is the stability of the threshold voltage (V_T) against a change in the gate length (l_g). I_d - V_d characteristics for the new devices with two different gate lengths are compared in Fig. 8. g_m increased from 125m S/mm to 180 mS/mm with decreasing lg from 2.2μm to 1.2μm, but V_T is almost the same. The V_T dependence on lg for the newly developed GaAs MESFETs is shown in Fig. 9, in comparing with that for the devices with n^+ implanted regions. It was verified by the experimental results that the new device exhibits a much smaller short channel effect than those with n^+ source and drain regions, giving a stable and reproducible operation, even for the submicron gate region.

§4 Summary

A novel device technology was developed, employing a sidewall SiO_2 on the gate electrode for the isolation of the electrodes. The new device exhibited a much larger transconductance than the conventional closely spaced electrode device. Moreover, the device can operate stably and reproducibly even for the submicron gate region, because of the reduced short channel effect which is a serious problem for a device with n^+ regions.

(a)

(b)

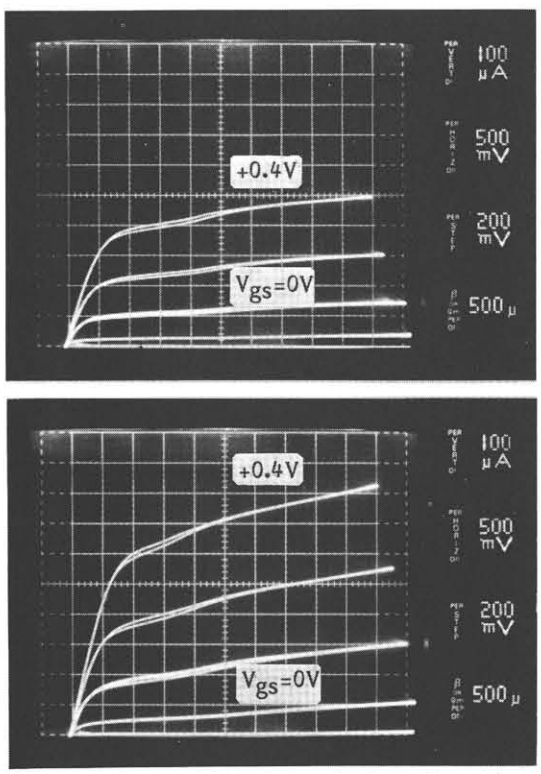

Fig. 8 I_d - V_d characteristics for the developed GaAs MESFETs with different gate lengths, (a) lg=2.2μm, (b) lg=1.2μm.

Acknowledgement

The authors wish to thank Y. Ogawa for her valuable technical assistance, and Dr. H. Muta for his continuous support and warm encouragement throughout this work.

This work is supported by the Agency of Industrial Science and Technology, MITI of Japan in the frame of the national research and development project "Scientific Computing System".

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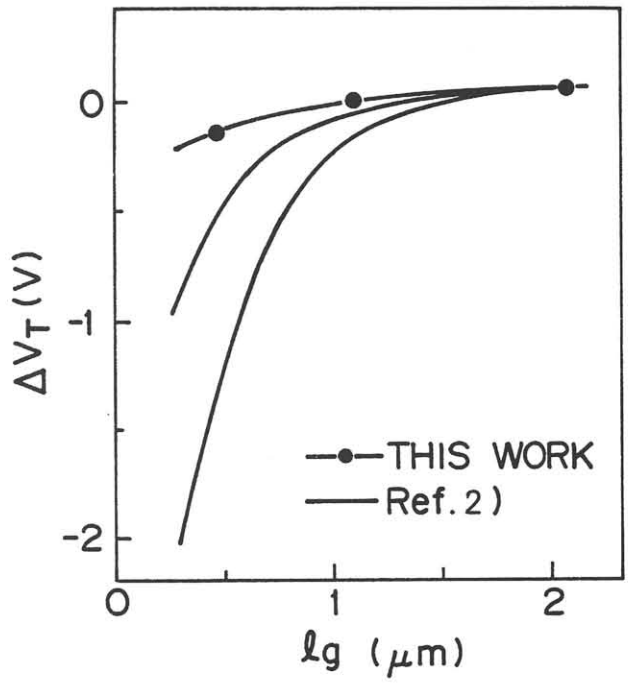

Fig. 9 Dependence of GaAs FET threshold voltage (V_T) on gate length (lg).