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A New GaAs MESFET with a Selectively Recessed Gate Structure

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We propose a new GaAs MESFET with a unique recessed gate structure. The structure is featured by the gate recess which is formed on the original surface of an MBE-grown GaAs active layer through selective etching of the over-grown n^+-$Ga_{1-x}Al_xAs$ source/drain layer. An excellent uniformity in the threshold voltage has been obtained over a 2"-diameter wafer. This result is attributed to the MBE-grown uniformity of the active layer thickness which remains unchanged even after formation of the gate recess. The new FET structure also offers a low source resistance because of heavy doping in the $Ga_{1-x}Al_xAs$ layer.

A variety of new processes and device structures have recently been studied for implementing the GaAs LSI's.[(1),(2)] High uniformity of device parameters over a wafer is essentially required for fabrication of GaAs LSI's.

In this paper, we propose a new structure for a GaAs MESFET with a recessed gate, of which depth can be self-controlled by selective etching of the hetero-epitaxial layer. The new structure FET's fabricated on a substrate exhibited very high uniformity in device characteristics. A low source resistance is also provided because of the heavily doped source/drain layer.

Figure 1 shows the schematic crosssection of the new FET structure. This structure is featured by the uniformly recessed gates which are implemented utilizing selective etching for the $Ga_{1-x}Al_xAs$/GaAs hetero-epitaxial layer. The preferential etching of $Ga_{1-x}Al_xAs$ to GaAs automatically stops at the interface, so that the thickness of the GaAs active layer can maintain the original as-grown uniformity. As a result the electrical characteristics of the FET's fabricated from one wafer will distribute in a very narrow range of fluctuation. It is also to be noted that the new FET structure offers a low source resistance because the $Ga_{1-x}Al_xAs$ layer for the source/drain region can be heavily doped with a donor impurity independently of the doping level in the GaAs active layer.

In order to obtain high uniformity in the

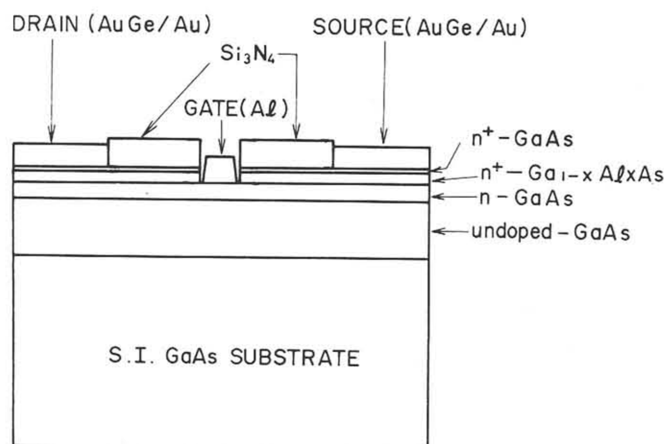

Fig. 1 Schematic crosssection of the new FET structure.

layer thickness and doping profile over a wafer, we have used the molecular beam epitaxy (MBE) technique with the PHI MBE/425M system. The uniformity obtainable with our system was preliminarily tested by measuring the thickness of an aluminum film grown on a 3 inch silicon substrate. The measured deviations of the film thickness throughout the wafer are within $\pm 2\%$.

For fabrication of the new structure FET devices, four layers were successively grown on a Cr-doped 2-inch (100) semi-insulating GaAs substrate; a 2.0μm thick undoped GaAs buffer layer, an n-GaAs ($\simeq 1\times10^{17} cm^{-3}$) active layer, an 0.17μm

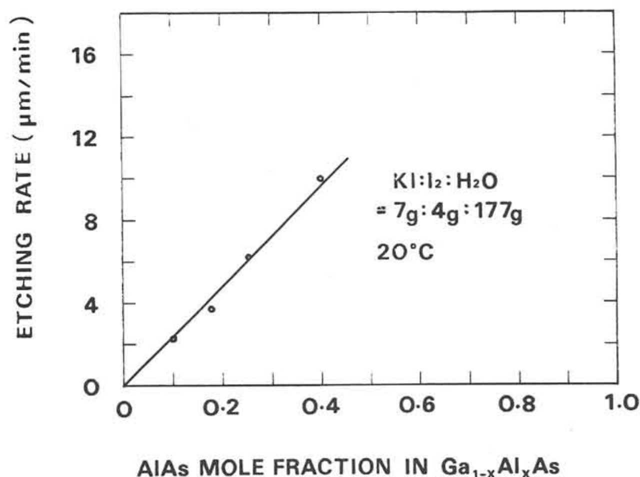

Fig. 2 Dependence of the etching rate for $Ga_{1-x}Al_xAs$ on the AlAs mole fraction x.

thick n^+-$Ga_{0.74}Al_{0.26}As$ ($\simeq$ $8x10^{17}$ cm^{-3}) source/drain layer and an 0.01μm thick n^+-GaAs ($\simeq$ $1x10^{18}$ cm^{-3}) cap layer. Silicon was employed as the n-type dopant. The temperature of the substrate, which was rotated continuously at 2 rpm, was kept at 580°C during GaAs growth and at 680°C during $Ga_{0.74}Al_{0.26}As$ growth. The typical growth rate was 1.0μm/H for GaAs and 1.2μm/H for $Ga_{0.74}Al_{0.26}$ As. The thickness of the n-GaAs active layer grown is 0.09μm thick for the normally off enhancement-mode FET (E-FET) and 0.3μm for the normally on depletion-mode FET (D-FET).

The active region of the FET was defined by mesa-etching. AuGe/Au filmes were evaporated and lifted off for the source/drain electrode. Alloying was perfomed at 500°C in a H_2 ambience before the gate formation. The gate-recesses were formed by selective etching of the $Ga_{0.74}Al_{0.26}As$ layer through the Si_3N_4 windows using an iodine solution; $KI:I_2:H_2O$=7g:4g:177g. Figure 2 shows the dependence of the etching rate of this etchant for $Ga_{1-x}Al_xAs$ on the AlAs mole fraction x. The rates of etching $Ga_{0.74}Al_{0.26}As$ for the source/drain region and GaAs for the active region are 6μm/m and 0.01μm/m, respectively, so that the etching of the gate region can automatically stop at the interface. The aluminum gates of 1.2μm (L) x 20μm (W) was defined by the lift-off technique.

Figure 3 shows the surface photograph of the processed 2 inch GaAs wafer. Figure 4 shows the SEM photograph of a cleaved crosssection of the fabricated FET. The typical characteristics of the E-FET and D-FET are shown in Fig. 5 and Fig. 6, respectively. The transconductances, gm's were measured to be 0.6mS (+0.6V gate biased) in the E-FET and 1.9mS (0 biased) in the D-FET, namely 30mS/mm and 95mS/mm, respectively.

The experimental devices over a wide area of the substrate showed highly uniform FET characteristics. The distributions of the threshold voltage V_T measured on a 2 inch diameter wafer of the E-FET's and D-FET's are shown in Fig. 7 and Fig. 8, respectively. For the E-FET's the mean value $\bar{x}$ and the standard deviation of distribution σ are +0.08V and 0.016V, respectively and for the

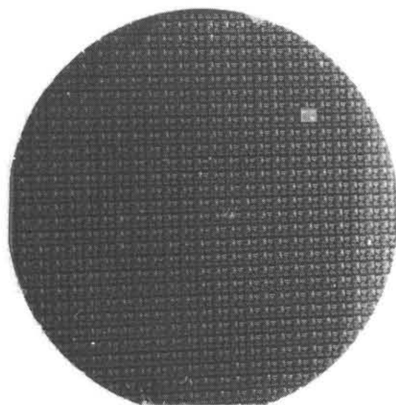

Fig. 3 Surface photograph of the processed 2 inch GaAs wafer.

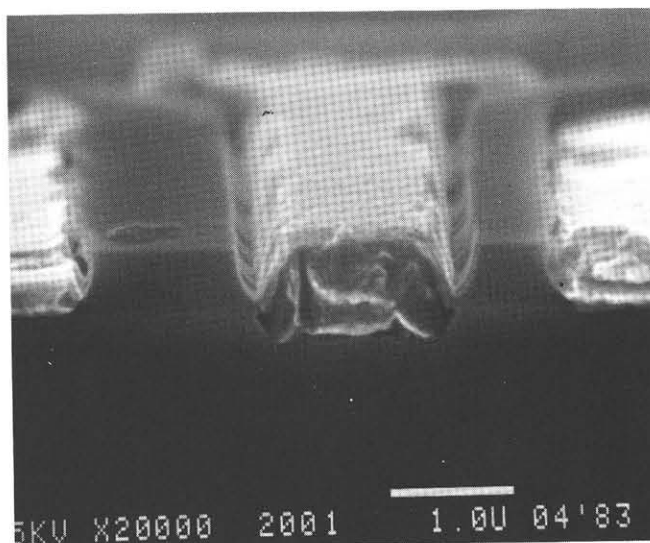

Fig. 4 SEM photograph of a cleaved crosssection of the FET.

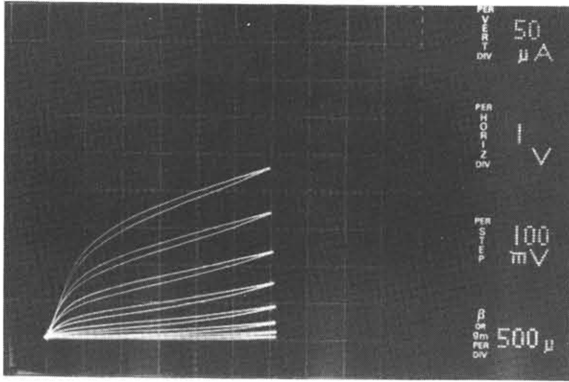

Fig. 5 Typical I_{DS}-V_{DS} curves of the fabricated E-FET; gate voltage, 0.1V/step from 0.0 to 0.7V.

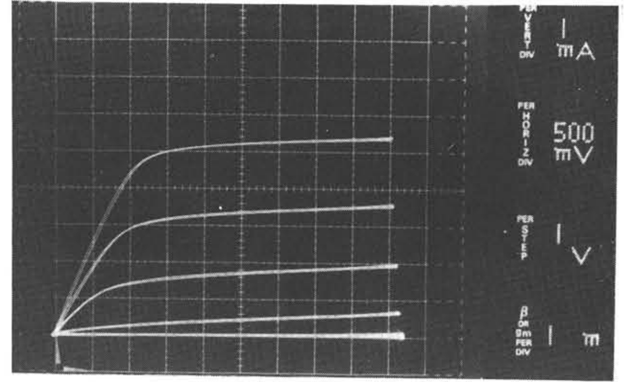

Fig. 6 Typical I_{DS}-V_{DS} curves of the fabricated D-FET.

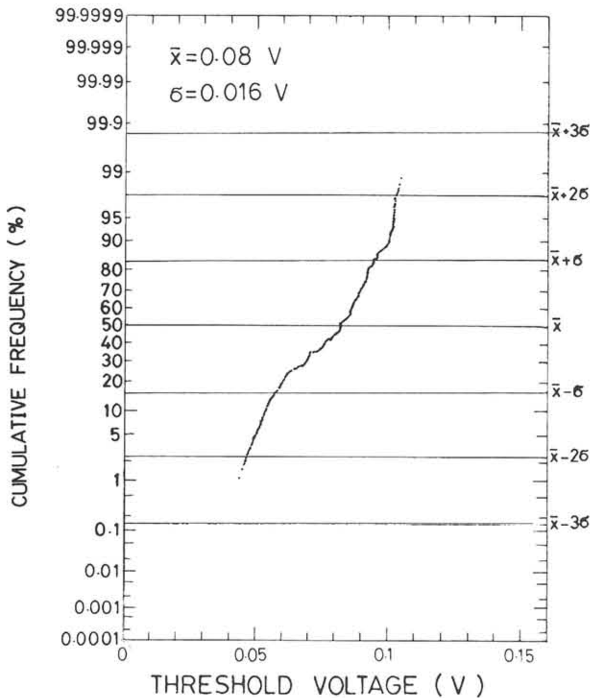

Fig. 7 Distribution of the threshold voltage of the E-FET's.

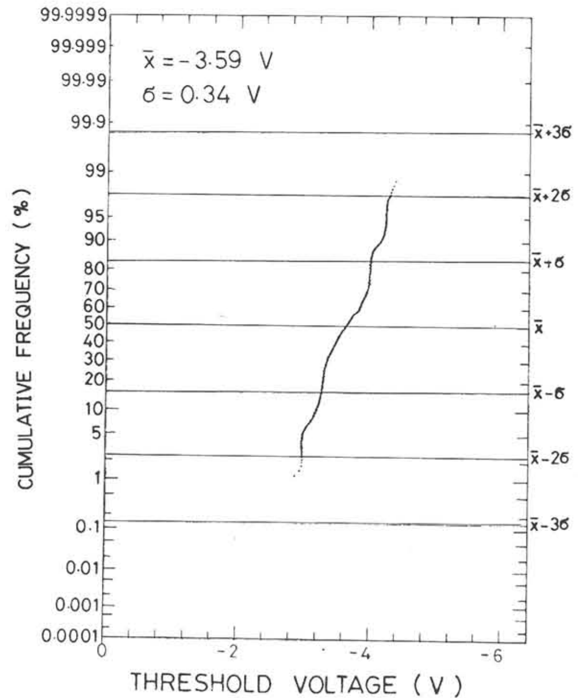

Fig. 8 Distribution of the threshold voltage of the D-FET's.

D-FET's -3.59V and 0.34V, respectively. These data indicate that the significantly higher uniformity of the threshold voltage than that of conventional recessed gate FET's or implanted FET's[3] was successfully obtained. This excellent uniformity is obviously attributed to the MBE-grown uniformity of the active layer thickness which remains unchanged even after formation of the gate recess.

The measured gate-source resistance of a D-FET is 56 Ω, namely 1.12 Ω/mm, which is about 70% smaller than that of the conventional recessed gate MESFET and is almost equal to that of the ion-implanted self-aligned FET with the same design.

In summary, the new GaAs MESFET with a selectively recessed gate structure has been demonstrated. The distribution of the threshold voltage of the devices fabricated on a 2 inch dia-

meter is found to be extremely uniform over a wafer. It has also been shown that the low source-gate resistance is inherent in the present new structure.

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