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Device Model for Ion-Implanted GaAs MESFET Including Compensation Mechanism of SI Substrate

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A device model for ion-implanted GaAs MESFET including compensation mechanism of semi-insulating substrate is presented. Calculation based on this model predicts that closely compensation of Cr and EL2 is desirable to reduce backgating. Experimental results require consideration of substrate leakage to understand backgating.

I. Introduction

GaAs MESFET's fabricated by ion-implantation into Cr doped or undoped semi-insulating (SI) substrate have been widely used for high speed digital and analog integrated circuit's (IC's). Semi-insulating GaAs substrate provides good isolation between the devices and minimizes the parasitic capacitance in the circuit. However, depending on the types of SI GaAs, the device characteristics can be strongly influenced by the properties of the substrate. Backgating effect is one of the substrate related effects which can not only degrade device performance, but also may give ultimate limitation to the achievement of densely packed, large scale integration of GaAs FET's. Understanding the physical mechanism of the effect, and controlling it are therefore strongly desired.

In spite of a number of experimental investigations on backgating effect and deep-level-spectroscopic studies[1),3)] to evaluate the substrate materials, direct connection between the compensation mechanism of substrate and the device characteristics is still left unclarified.

In this paper, an attempt to formulate a device model is presented, in which material parameters characterizing substrate compensation determine the space charge density at n-i junction region, and the modulation of FET characteristics by the backgate bias voltage can be evaluated numerically. Based on this model, discussions will be made indicating the guideline for the impurity compensation in SI substrate materials.

II. Device Model[2)]

Consider the ion-implanted GaAs MESFET with backgate electrode shown in Fig.1.

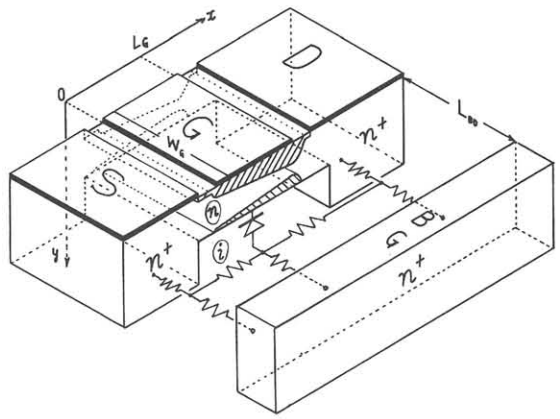

Fig.1 Bird's eye view of GaAs MESFET with backgate electrode. Depletion layer is formed between active layer and the substrate. Resistor network represents substrate which causes voltage drop when backgate bias is applied.

Appearance of electric dipole layer at the implanted channel and SI substrate interface n-i junction is inevitable because of the band bending and the partial ionization of trap levels (Fig.2).

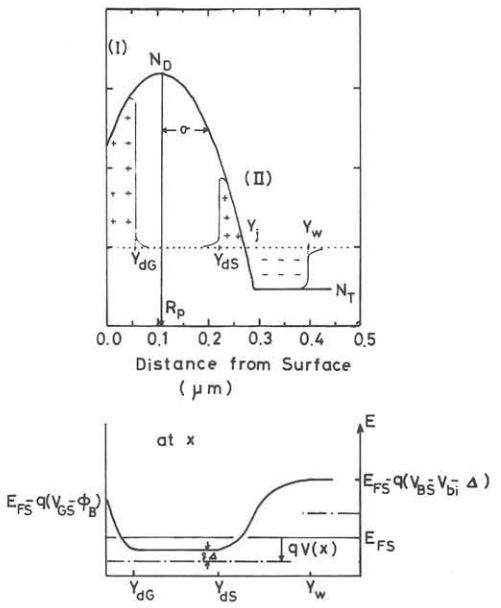

Fig.2 Appearance of electric dipole layer at the channel and SI substrate interface.
(a) Space charge distribution. Y_{dG} represents the depletion edge under gate and Y_{dS} channel side depletion edge, respectively.
(b) Band diagram at x = x. Energy and voltage are measured with respect to the Fermi level at the source end E_{FS}.

If we assume a 4-level model for compensation mechanism including EL2, chromium, shallow donor N_d and shallow acceptor N_a, the net concentration of negative charge on the substrate side of the depletion region N_{Teff} depends on the occupancy of the deep levels in the bulk according to the following relationship.[3]

$$N_{Teff} = N_{Cr}\left(\frac{e_{pCr}}{e_{nCr}+e_{pCr}} - \frac{1}{1+\exp\left(\frac{E_{Cr}-E_F}{kT}\right)}\right) + N_{EL2}\left(\frac{e_{pEL2}}{e_{nEL2}+e_{pEL2}} - \frac{1}{1+\exp\left(\frac{E_{EL2}-E_F}{kT}\right)}\right). \quad (1)$$

Given the voltage drop across the n-i junction V'_{BS}, the position of depletion edge Y_{dG} is determined by solving Poisson equation containing the fixed charge of eq. (1) and the implanted shallow ions:

$$N(y) = \frac{Q}{\sqrt{2\pi}\,\sigma}\exp\left[-\left(\frac{y-R_p}{\sqrt{2}\,\sigma}\right)^2\right] - N_{Teff} \quad (2),$$

where

Q : Dose [Ions/cm^2]

R_p : Projected Range [cm]

σ : Standard Deviation [cm]

(vertical problem).

The static FET characteristics are calculated as follows, considering the channel width constriction due to depletion layer formation (lateral problem).

In eq.(3), Y_{dG} is the depletion edge under gate and Y_{dS} is the depletion edge of the channel side (Fig.2).

$$I_{DS} = qW_G\int_0^{V_{DS}}\int_{y_{dG}(V(x))}^{y_{dS}(V(x))} n(y)\,dy\,\frac{\mu\frac{1}{L_G}}{1+\mu\frac{V_{DS}}{L_G v_s}}\,dV \quad (3),$$

Here velocity saturation mechanism is taken into account.

Channel current I_{DS} is then given by the following equations.

$$I_{DS} = \frac{q\mu\frac{Q}{2}\frac{W_G}{L_G}}{1+\frac{\mu V_{DS}}{v_s L_G}}\left\{(1+\alpha)V_{DS} - \frac{2}{3}V_1\left[\left(a_p^2+\frac{V_{DS}-V_P}{V_1}\right)^{\frac{3}{2}} - \left(a_p^2-\frac{V_P}{V_1}\right)^{\frac{3}{2}}\right] - \frac{2}{3}V_2\left[\left((\alpha+1-a_p)^2+\frac{V_{DS}-V_P}{V_2}\right)^{\frac{3}{2}} - \left((\alpha+1-a_p)^2-\frac{V_P}{V_2}\right)^{\frac{3}{2}}\right]\right\}, \quad (4)$$

where α, V_1, V_2 and a_p are defined by

$$\alpha = \frac{R_P}{2\sigma}\sqrt{\frac{\pi}{2}},\quad V_1 = \frac{qQ^2}{8N_{Teff}\varepsilon},\quad V_2 = \frac{qQ\sigma}{\sqrt{2\pi}\,\varepsilon},$$

$$a_p = \frac{2N_{Teff}}{Q}\frac{2\varepsilon}{qN_{Teff}}(V_{bi} - V'_{BS} + V_P).$$

As for the pinch-off voltage V_p or threshold voltage V_T is expressed as

$$V_T = \phi_B - \Delta - \frac{qQR_P}{2\varepsilon}\left[\operatorname{erf}\left(\frac{R_P}{\sqrt{2}\,\sigma}\right) + 1 - \frac{2N_{Teff}}{Q}\sqrt{\frac{2\varepsilon}{qN_{Teff}}(V_{bi}-V'_{BS})}\right] - \frac{qQ\sigma}{\sqrt{2\pi}\,\sigma}\left[\exp\left(-\frac{R_P^2}{2\sigma^2}\right) - \frac{4N_{Teff}}{Q}\sqrt{\frac{2\varepsilon}{qN_{Teff}}(V_{bi}-V'_{BS})} + \frac{8N_{Teff}\varepsilon}{qQ^2}(V_{bi}-V'_{BS})\right]. \quad (5)$$

In the above equations parameters are listed as follows.

Δ : $E_c - E_f$ at the source end [eV],

ϕ_B: barrier height of the Schottky gate [eV].

The numerical evaluation of fixed charge density of eq.(1) is shown in Fig.3. Heavy compensation by chromium results in larger value of interface charge while close compensation reduces N_{Teff}.

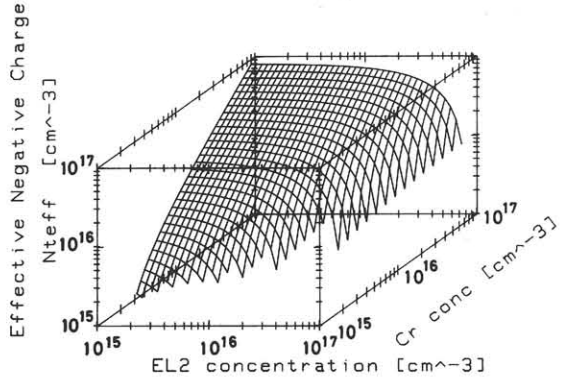

Fig.3 Evaluation of effective negative charge in the substrate side of the depletion region through eq.(1).

Some example of calculated backgating effect on I-V characteristics is shown in Fig.4(a). For typical values of V'_{BS} of -0.5 V already reduces I_{DS} appreciably.

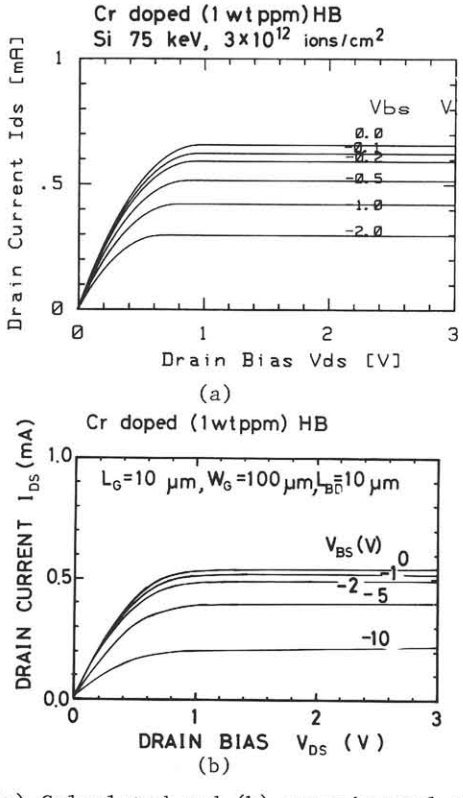

Fig.4 (a) Calculated and (b) experimental results of I-V characteristics with various values of backgate bias voltage V_{BS}.

In Fig.5 dependence of I_{DSS} on deep trap concentration and on V'_{BS} calculated from the model is shown.

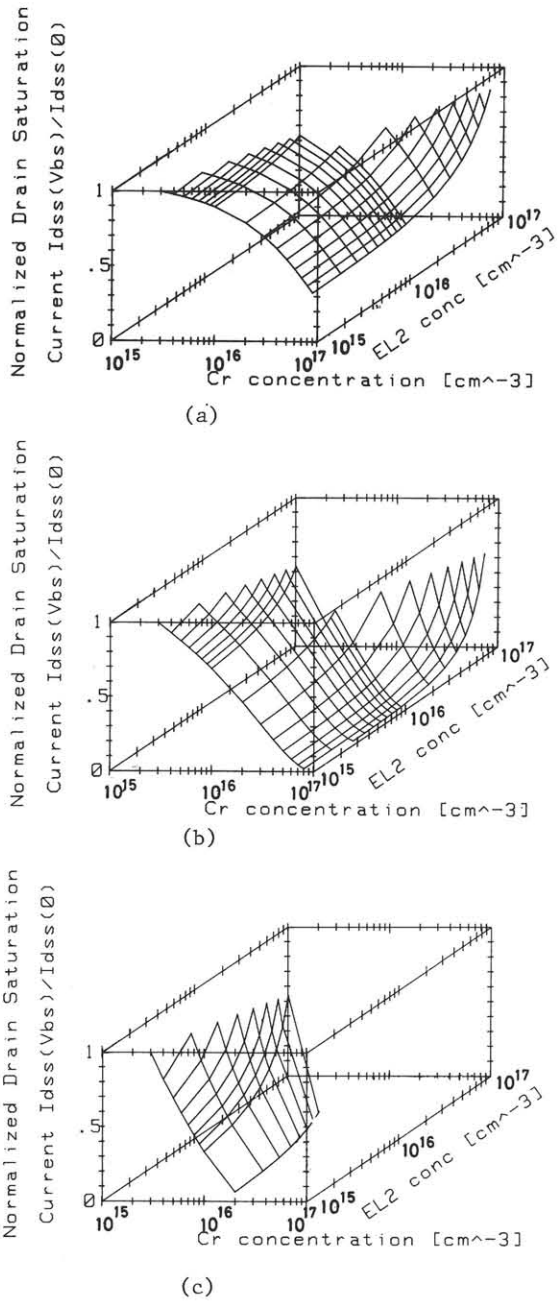

Fig.5 Dependence of I_{DSS} on deep trap concentration and effective backgate voltage V'_{BS}. (a) V'_{BS}=0 V, (b) V'_{BS}=-1 V and (c) V'_{BS}=-5 V, respectively.

Figure 5 also suggests that light compensation by Cr and EL2 can minimize backgating effect.

III. Comparison with experiment

The test devices fabricated by Si ion-implantation into Cr doped HB grown substrate were investigated. Implantation condition is that dose energy is 75 KeV and ion dose is 3×10^{12} cm^{-2} of Si. The FET has a gate 10 μm in length and 100 μm in width; the backgate electrode is placed with various distance ranging between 10 μm and 100 μm.

Examples of backgating effect and backgate leakage current are shown in Fig.4(b), Fig.6, respectively.

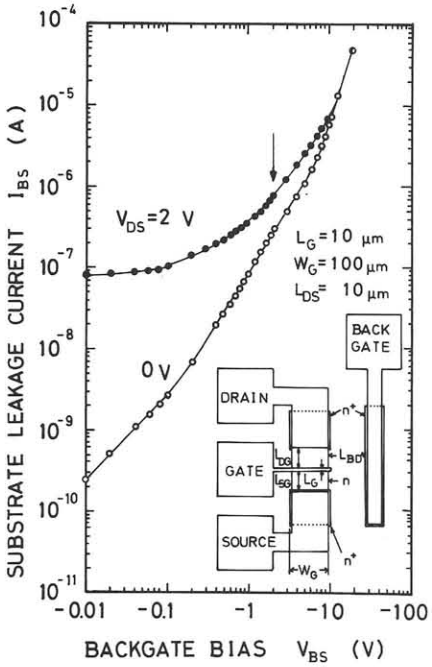

Fig.6 Backgate leakage current with V_{DS}=0 V and 2 V. Drain saturation current I_{DSS} is reduced to 90% of its initial value when V_{BS} is -2 V (indicated by an arrow). This result does not show any kink corresponding to the onset of backgating.

The leakage current does not show any kink nor have threshold voltage coincident with the beginning of the backgating, differing from the observation by C.P.Lee[4].

The leakage current causes voltage drop and the voltage across n-i junction V'_{BS} is much smaller than applied voltage V_{BS} (Fig.4(a) and (b)).

The external backgate bias voltage V_{BS}=-2 V causes 10% reduction of I_{DSS} when the backgate electrode is separated by 10 μm from the device. While in the FET with 100 μm separation, 10% reduction of I_{DSS} appears when V_{BS} is around -20 V. This fact indicates that V_{BS} causing same amount of current reduction is nearly proportional to the distance between the backgate electrode and the device. Therefore, it is natural to take that the backgate bias voltage is devided into two portions, that is, V'_{BS} which is applied to the n-i junction and the voltage drop $V_{BS}-V'_{BS}$ through the substrate.

IV. Summary

We formulated a model for an ion-implanted GaAs MESFET including compensation mechanism of a SI substrate. This model suggests that close compensation of EL2 and Cr is desirable from the standpoint of reduction of backgating. From the experimental results, substrate leakage current analysis is necessary to understand the backgating thoroughly.

Acknowledgement

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