Invited

Substrate Materials for GaAs Integrated Circuits

C.G.Kirkpatrick, R.T. Chen, D.E. Holmes, K.R. Elliott and P.M. Asbeck

Rockwell International
Microelectronics Research and Development Center
Thousand Oaks, CA 91360 USA

Recent progress in the characterization, growth and application of LEC (Liquid Encapsulated Czochralski) undoped semi-insulating GaAs for integrated circuit fabrication at our laboratory is presented. Approaches for qualifying GaAs materials for digital IC processing, improving the yield of semi-insulating substrates and reducing dislocation densities are described. The successful application of these materials to MESFET device fabrication is discussed, as well as implementation in HEMT (high electron mobility transistor) and HBT (heterojunction bipolar transistor) epitaxial growth, is discussed.

INTRODUCTION

Significant improvements in the quality, size, and supply of semi-insulating GaAs substrates are now making GaAs device production a reality. In particular, the Liquid Encapsulated Czochralski (LEC) technique[1-5] for the growth of large, round GaAs crystals, has facilitated the development of GaAs processing, to the extent that device manufacturing activities are feasible. In this paper, the progress in the growth and selection of GaAs materials for digital device applications attained in our laboratory will be discussed. The resulting impact of undoped, semi-insulating large wafers on GaAs device fabrication will be described.

MATERIAL QUALIFICATION

Variability in the electrical and crystalline characteristics of GaAs substrates available in the past, in particular those grown by the Bridgman technique and doped with chromium, mandated the application of material qualification or selection techniques before use in device fabrication. The specifications we utilize to select GaAs substrates for digital integrated circuit fabrication include high resistivity, good activation of implanted dopants, dislocation density and crystalline perfection requirements, and dimensional and flatness criteria.

At present, we utilize 3-inch (100) undoped, semi-insulating substrates in our digital research and development activities as well as our pilot line work. This includes devices based on MESFETs (metal-semiconductor field effect transistors), HEMTs (high electron mobility transistors), and HBTs (heterojunction bipolar transistors). The 3-inch round wafer format was selected to facilitate use of standard semiconductor processing equipment. A major and minor flat are utilized, to uniquely orient each wafer with respect to the two non-identical planes in each (100) wafer, which can effect the threshold voltage in FETs[6]. Relatively thick (25 mil) wafers with edge beveling are used in device processing to minimize breakage. A featureless, flat wafer surface is sought, to maximize yields in lithography.

Evaluation of the electrical characteristics of semi-insulating substrates for device fabrication applications is particularly important for high yields and performance. This is particularly the case for structures which utilize the semi-insulating substrate directly in the formation of device active layers, such as GaAs MESFETs (Fig. 1). In these devices, the high resistivity substrate functions as the isolation between devices, and the active layers are formed by individual ion implantation steps directly in the substrate. The thermal stability of substrates used in ion implantation processing is particularly critical, since the annealing steps which follow to activate dopants and remove radiation damage, can result in the formation of conducting skins on the wafer surface for some materials. GaAs materials made semi-insulating through the addition of compensating dopants such as chromium are particularly susceptible to such changes. Thermal processing can cause redistribution of the chromium[7,8]. If the background of donor impurities (usually Si) is sufficiently high, an uncompensated surface conducting layer is formed, making the material unsuitable for device fabrication utilizing the substrate for isolation. In addition, this effect can manifest itself in the carrier profile of the lightly doped channel layer of the FET as shown in Fig. 2.

While the application of undoped, semi-insulating LEC substrates has largely eliminated these problems, careful evaluation of the implant activation and profile, as well as the substrate resistivity before and after annealing, is carried out to ensure only materials which display standard properties are utilized in device fabrication. Materials for HEMT and HBT processing undergo essentially the same screening process. Undoped LEC materials are used as substrates for molecular beam epitaxy (MBE) layer

growth for these devices[9,11], to minimize the possibility of impurity outdiffusion into epitaxial layers.

LEC GROWTH

All of the materials presently used to fabricate digital ICs in our laboratory are produced by high pressure LEC growth techniques. In-situ synthesis is utilized to compound GaAs inside the puller just prior to growth. Through this and the use of high purity (6-9s) starting materials, the introduction of contaminants into the melt is minimized. The boric oxide wetting the crucible and floating on top of the melt, together with the inert gas overpressure, encapsulate the melt to maintain stoichiometry. A seed is then dipped into the melt through the boric oxide to commence growth. The crystal diameter is controlled manually or with the aid of a microprocessor, by adjusting the temperature and cooling rate in response to variation in the crystal's differential weight. The differential weight signal is provided by a "load cell" which weighs the crystal. Typical crystals will weigh 2-4 kilograms, and produce 50-150 wafers.

ELECTRICAL CHARACTERISTICS

When pyrolytic boron nitride (PBN) crucibles are utilized together with high purity starting materials, the resulting undoped materials display very high purity[12,3,5]. The levels of background impurities in undoped, semi-insulating LEC GaAs grown in our laboratory are determined by secondary ion mass spectroscopy (SIMS) and localized vibrational mode (LVM) far-infrared absorption. The data indicate that concentrations of most impurities are quite low (near the sensitivity limits of the analysis tools), except for boron (B) and carbon (C). Boron is isoelectronic in GaAs and does not apparently contribute electrically to the material. Carbon, however, can act as an acceptor.

Detailed characterization of the impurities present in undoped LEC GaAs, together with investigations on stoichiometry-related centers in the materials, have resulted in improved understanding of the compensation mechanism in undoped materials and of means to control the resistivity. The results of our investigations [4,13-15] are shown in Fig. 3. Crystals were grown from Ga-rich, As-rich, and near stoichiometric melts. The electrical properties of the resulting materials were evaluated by room temperature and variable-temperature Hall effect measurements, room temperature optical absorption, and photoluminescence. The electrical properties of undoped material are controlled by the melt stoichiometry as a consequence of the presence of EL2 deep donors, 77 meV acceptors, and carbon acceptors, as shown in Fig. 3. Semi-insulating material is obtained above a critical melt composition. The free electron concentration in the semi-insulating material is controlled by the balance between EL2 deep donors and residual (uncompensated) carbon. The dependence of the concentrations of EL2 and the 77 meV acceptors on melt stoichiometry strongly suggests that these centers are native defects.

While this model provides the basic recipe for the high yield growth of undoped, semi-insulating materials, additional fine tuning of the electrical properties of these substrates is desirable for uniformity and reproducibility in IC device parameters. The effect[16] of the residual carbon concentration on the threshold voltage of FETs fabricated by direct ion implantation into undoped semi-insulating LEC GaAs is shown in Fig. 4. The threshold voltage decreases linearly as the carbon concentration increases. No such correlation between the threshold voltage and EL2 is observed, however.

The distribution of carbon concentrations over 3-inch undoped GaAs wafers has been investigated[16], as shown in Fig. 5. The variations are relatively modest in our materials, indicating reasonable degrees of uniformity in the threshold voltage might be expected. This is verified by the data of Fig. 6, which shows the excellent uniformity observed for FET threshold voltage across a nearby 3-inch wafer.

The distribution of EL2 over 3-inch wafers has also been studied[17,18], to produce quantitative contour maps on undoped LEC GaAs. Correlation between EL2 and dislocation distributions is observed for seed-end wafers, as shown in Fig. 7. Asymmetric EL2 patterns are, however, observed in the tail region. The variations in EL2 are believed to be controlled by stress induced dislocation climb in the crystal.

CRYSTALLINE CHARACTERISTICS

While LEC GaAs materials display significantly fewer crystalline faults such as precipitates, inclusions, and twins, than materials produced by horizontal growth techniques, the levels of dislocation densities observed in these materials are relatively high. Although we have not observed a direct impact of dislocation density on the yield of digital ICs, even in complex circuits, concern over the possible impact on performance and reliability provided the impetus for a substantial in-house growth effort aimed at reducing dislocation densities. The effects of seven growth parameters on the dislocation density and distribution were investigated[19]. These were: (1) cone angle, (2) seed quality, (3) seed necking, (4) diameter control, (5) melt stoichiometry, (6) height of the boric oxide encapsulating layer, and (7) ambient pressure.

From experiments varying the growth cone angle from 0° to 70°, we found that a 30° cone angle allowed minimum dislocation density growth, while increasing the full diameter growth region. The dislocation density in the front of the crystals was a strong function of the height of the encapsulating layer, decreasing as the layer height increases. Lower ambient pressures are also effective in reducing the dislocation density, although care must be exercised to prevent surface degradation of the crystal. Dash-type seed necking is effective in reducing the dislocation density only when the EPD of the seed is high (greater than 5000 cm^{-2}); low dislocation crystals are grown with poor quality seeds with necking and with high quality seeds with and without necking. In addition, good diameter control, and the use of

slightly As-rich melts favor reduced dislocation densities; these parameters also favor twin-free growth.

With these techniques, the best dislocation density result we have observed in 3-inch undoped LEC materials is 6000 cm^{-2}. More typically, dislocations range from 10-50,000 cm^{-2} on 3-inch wafers. Purchased materials with substantially higher dislocation densities have, however, been successfully applied to digital IC MESFET processing without noticeable impact on yield or performance.

DEVICE APPLICATIONS

As indicated in Fig. 6, the uniformity of undoped semi-insulating GaAs is excellent for ion implantation processing. The resulting uniformity in device parameters has allowed successful fabrication of low power and high speed (1 nsec access time) 256 bit RAM devices and 8-bit by 8-bit (1008 gate) multiplier circuits. In addition, these same undoped LEC GaAs materials have been utilized to fabricate heterojunction bipolar devices with cutoff frequencies as high as 16 GHz[10], and HEMT inverters with 12.2 psec propagation delay[11].

SUMMARY

Significant improvements in the size, electrical characteristics, crystalline features, and supply of semi-insulating GaAs materials for IC applications have resulted from the development of the high pressure LEC growth technique. Understanding of the compensation mechanism in undoped, semi-insulating material, together with the utilization of techniques to reduce dislocation densities and twins, have significantly improved material quality and availability. The existence of a reliable supply of GaAs substrates for IC fabrication is facilitating the move of this high performance technology from the laboratory into manufacturing. LEC materials, with uniform sizes conforming to standard semiconductor processing equipment, as well as thermal stability and high purity, are excellent substrates for ion implantation based processing, as well as epitaxial based technologies. Continued improvements will continue to be sought to control substrate parameters which affect device parameters, and reduce and homogenize dislocation densities.

ACKNOWLEDGMENTS

REFERENCES

1. E.M. Swiggard, S.H. Lee, and F.W. Von Batchelder, Inst. Phys. Conf. Ser. # 336, 23 (1977). See also R.L. Henry and E.M. Swiggard, Inst. Phys. Conf. Ser. # 336, 28 (1977).
2. T.R. AuCoin, R.L. Ross, M.J. Wade and R.O. Savage, Solid State Tech. 22(1), 59 (1979).
3. D.E. Holmes, R.T. Chen, K.R. Elliott and C.G. Kirkpatrick, Appl. Phys. Lett. 40, 46(1982).
4. D.E. Holmes, R.T. Chen, K.R. Elliott, C.G. Kirkpatrick and P.W. Yu, IEEE Trans. MTT-30, 949 (1982).
5. R.D. Fairman, R.T. Chen, J.R. Oliver and D.R. Ch'en, IEEE Trans. Electron Devices, ED-28, 135 (1981).
6. C.P. Lee, R. Zucca and B.M. Welch, Appl. Phys. Lett. 37, 311 (1980).
7. P.M. Asbeck, J. Tandon, E. Babcock, B. Welch, C. Evans, and V. Deline, IEEE Trans. Electron Devices, ED-26, 1853 (1979).
8. B. Tuck, G.A. Adegoboyega, P.R. Jay and M.J. Cardwell, in Gallium Arsenide and Related Compounds, Inst. Phys. Conf. Ser. # 45, 114(1978).
9. P.M. Asbeck, D.L. Miller, R.A. Milano, J.S. Harris, Jr., G.R. Kaelin and R. Zucca, IEEE IEDM Technical Digest 629 (1981).
10. D.L. Miller, P.M. Asbeck, R.J. Anderson and F.H. Eisen, Electronics Lett. 19, 367 (1983).
11. C.P. Lee, D.L. Miller, D. Hou and R.J. Anderson, 41st Device Research Conf., Burlington, VT, June 20-22, 1983.
12. J.R. Oliver, R.D. Fairman, R.T. Chen and P.W. Yu, Electronics Lett. 17, 839 (1981).
13. D.E. Holmes, K.R. Elliott, R.T. Chen and C.G. Kirkpatrick, in "Semi-insulating III-V Materials" (Shiva, England, 1982), p. 19.
14. P.W. Yu, D.E. Holmes and R.T. Chen, Inst. Phys. Conf. Ser. # 63, 209 (1981).
15. K.R. Elliott, D.E. Holmes, R.T. Chen and C.G. Kirkpatrick, Appl. Phys. Lett., 40,898(1982).
16. R.T. Chen, D.E. Holmes and C.G. Kirkpatrick, 25th Electronic Materials Conf., Burlington, VT., June 22-24, 1983.
17. D.E. Holmes, R.T. Chen, K.R. Elliott and C.G. Kirkpatrick, to be published in Appl. Phys. Lett., July 1983.
18. D.E. Holmes, R.T. Chen and C.G. Kirkpatrick, 25th Electronic Materials Conf., Burlington, VT., June 22-24, 1983.
19. R.T. Chen and D.E. Holmes, J. Crystal Growth 61, 111 (1983).
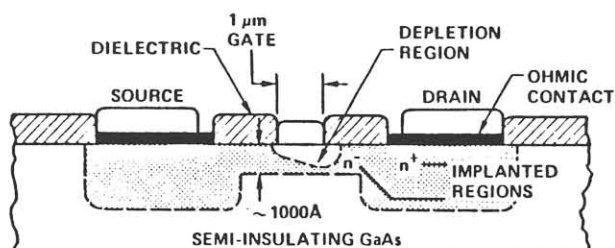
FIGURES

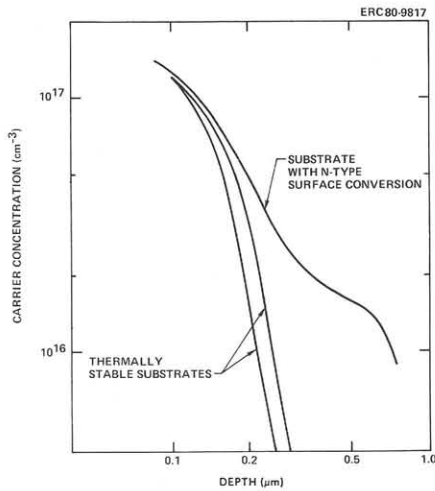Fig. 1. Cross section of MESFET structure formed by ion implantation into a semi-insulating substrate.

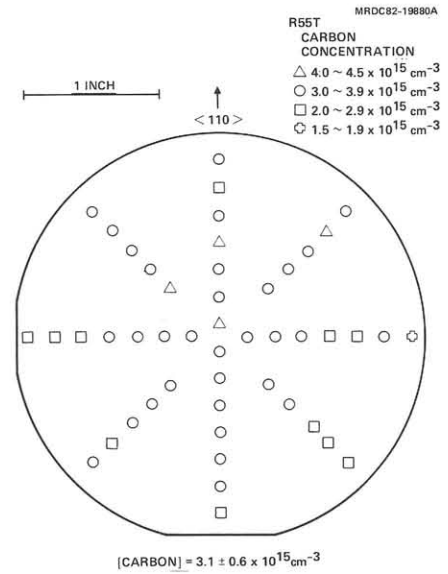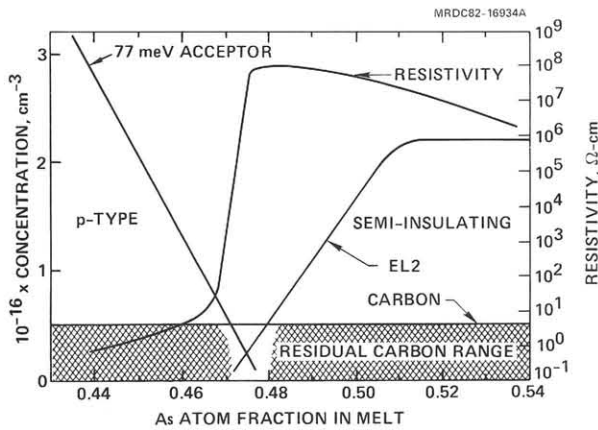Fig. 2. Carrier concentration profiles for ion implanted FET channel layers.

Fig. 3. Effect of stoichiometry on resistivity showing the relationship between carbon, EL2, and 77 meV traps on compensation.

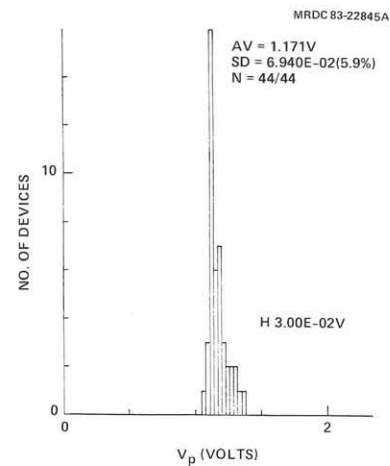Fig. 4. Plot of depletion voltage as a function of residual carbon concentration.

Fig. 5. Map of carbon concentration over 3-inch wafer.

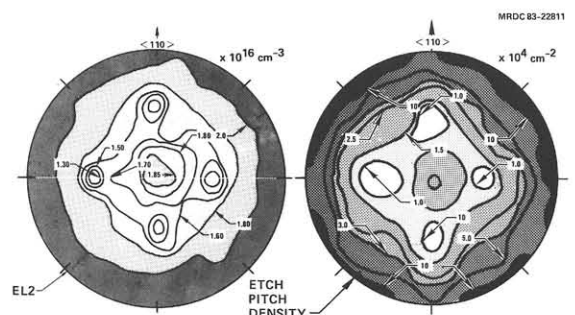Fig. 6. Uniformity of threshold voltage over 3-inch wafer.

Fig. 7. Correlation of EL2 and dislocation distributions at crystal seed-end.