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Amorphous Si:H Linear Image Sensor Operated by a-Si:H TFT Array

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A 64 bit a-Si:H linear image sensor operated by an a-Si:H TFT array has been proposed. This sensor consists of photodiode array, TFT array, matrix circuit and external circuit. TFT on resistance is approximately 400 kΩ and mobility is 0.6 $cm^2/V\cdot sec$ at 30 V gate voltage. 5 μsec read out time is obtained in the conventional matrix mode scanning. Moreover, a novel driving method is applied in order to improve effective operation speed. Experimental data confirm the validity of the concept.

1. Introduction

A large scale linear image sensor using amorphous Si is an attractive device for compact and high speed facsimile equipment because of its short photoresponse time and simplicity for fabrication.[1],[2],[3] However, since these sensors consist of an a-Si:H photodiode array and IC scanners, a large number of wire bondings and IC scanners are required. Fabricating switching devices and photodiodes on the same substrate avoids this manufacturing difficulty. K.Ozawa et al. have proposed a linear image sensor with blocking diode.[4] On the other hand, M.Matsumura et al. have proposed a linear image sensor combined with an a-Si:H thin film transistor (TFT) and obtained a good reproduced image operated at 300 Hz.[5] However, due to low a-Si:H TFT mobility, more than 100 μsec switching time is needed, which is too slow to be used in GIII mode facsimile (2.5μsec/bit).

In order to improve the operation frequency, we have developed a linear image sensor using a photodiode combined with high mobility TFT. Since the photodiode has short photoresponse time, this sensor can be scanned at high speed. Moreover, a novel driving method is applied.

2. Device Operation

Figure 1 shows the 64 bit linear image sensor fabricated and studied. This sensor consists of photodiode array, TFT array, matrix circuit and external circuit, which includes transfer capacitors Ci ($i=1\sim 8$) and analog multiplexer. TFTs are connected in an 8x8 row-column matrix. Each outlet terminal is connected to the transfer capacitor, a discrete capacitor, which transfers signal charge from the photodiode to a detection circuit. However, in the case of a large size linear image sensor, stray capacitance in the lines functions as the transfer capacitor.

The sensor operates as follows. Figure 2 shows the timing diagram. In the T_G period for ϕ_{Ti}, photo-charge, which are integrated in the photodiodes ($S_{i,1} \sim S_{i,8}$) during integration time Ti, are transfered into capacitors $C_1 \sim C_8$ simultaneously. After the TFTs turn off, the analog multiplexer reads out these charge during T_A of $\phi_{A1} \sim \phi_{A8}$. In this driving method, operation speed for one column is T_G+8T_A in the shortest case. Therefore, effective operation speed per bit τ is given by

$$\tau = (T_G + 8T_A)/8. \qquad (1)$$

In the conventional matrix mode scanning, operation speed is T_G. Reduction in the number of TFT switchings increases the operation frequency.

To explain operation speed for this sensor, consider the charge transfer speed from the photodiode to the detection circuit. Figure 3 shows the

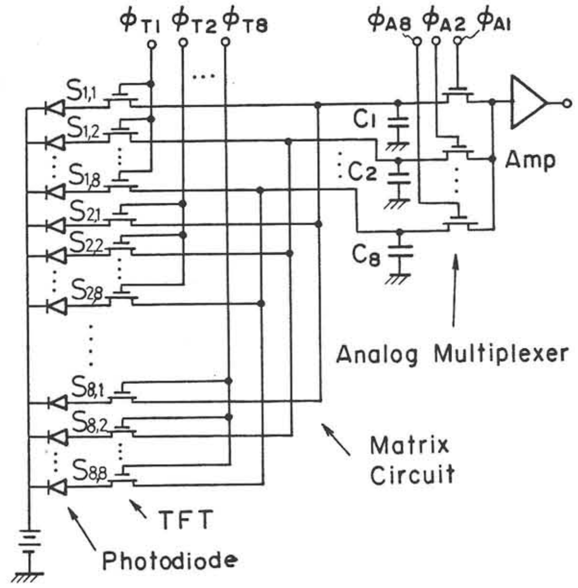

Fig.1 Equivalent circuit for 64 bit a-Si:H linear image sensor

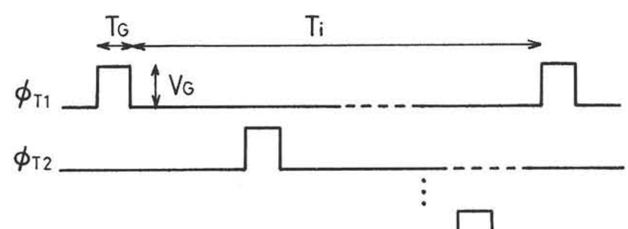

Fig.2 Timing diagram

equivalent circuit for charge transfer between photodiode and detection circuit. Ca is photodiode storage capacitance. Qa is photo-charge, which is generated by the photodiode during integration time Ti. R_T is TFT on resistance, R_A is analog multiplexer on resistance and Rin is input impedance for the detection circuit (Integrator). The charge trasfer equation in the T_G period is written as

$$Qa=Qi\frac{C_i}{C_i+C_a}(1-\exp(-\frac{C_i+C_a}{C_iC_aR_T}t)) \qquad (2)$$

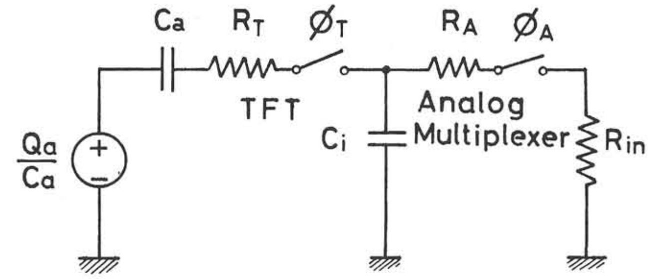

Fig.3 Equivalent circuit for charge transfer between photodiode and detection circuit

where Qi is charge at Ci. It is clear from Eq.(2) that Ci should be much larger than Ca in order to minimize afterimage.

When Ca<<Ci, Eq.(2) is rewritten as

$$Qa=Qi(1-\exp(-\frac{1}{C_aR_T}t)). \qquad (3)$$

Then the time constant is nearly equal to CaR_T.

At the next step, Qi is discharged by switching the analog multiplexer. The time constant is $Ci(R_A+Rin)$. In this sensor, R_A is 200 Ω and Rin is 500Ω, respectively. Since R_A and Rin are sufficiently small, T_A can be much samller than T_G. For example, when Ci is 300 pF, time constant is 0.21μsec. Even if T_G is 100μsec[5], operation speed per bit is approximately 13 μsec from Eq.(1). As a result, effective read out time per bit is greatly reduced, compared with conventional matrix mode scanning.

3. Device Structure and Fabrication

Figures 4 and 5 show a cross sectional view and photograph for this sensor, respectively. The photodiode has a sandwitch like structure with SiN_x and p-a-Si:H blocking layers on both sides of a photosensitive a-Si:H layer[3]. These blocking layers decrease dark current and provide high photosensitivity. The effective photosensitive area is 100μm x 100μm (8 bits/mm). The a-Si:H TFT configuration is inverted staggered structure. The gate insulator is SiN_x. A thin phosphorous-doped layer is deposited on top of the undoped layer as an ohmic contact to an evaporated Al electrode. Channel length and width are 20μm and 1 mm, respectively. Polyimide is used for a matrix

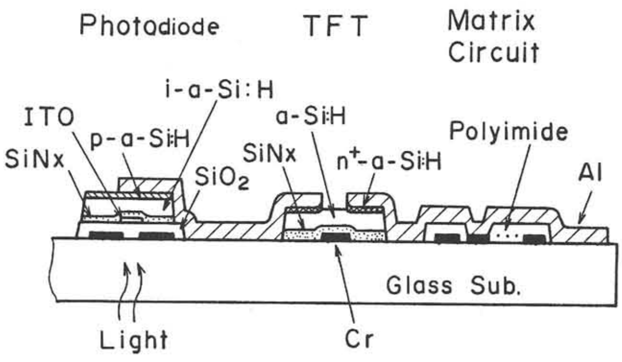

Fig.4 Cross sectional view of a-Si:H linear image sensor operated by a-Si:H TFT array

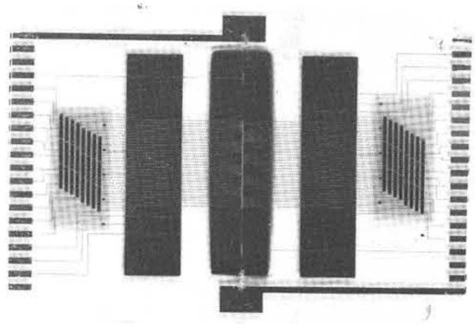

Fig.5 64 bit a-Si:H linear image sensor

circuit insulator. Fabrication procedures are as follows: A 1000 Å thick Cr film was first evaporated on Corning 7059 glass and formed into a light shield layer, gate electrode and lower electrode for matrix circuit. Polyimide was coated and chemically etched by photoetching process. A 0.5 μm thick SiO_2 film and a 400 Å thick transparent ITO film were deposited by rf sputtering. The ITO film was etched to form a 200 μm wide common electrode. To fabricate TFT, 0.3 μm thick SiN_x, 0.3 μm nondoped a-Si:H and 500 Å n^+-a-Si:H layers were deposited continuously. To fabricate the photodiode, 300 Å thick SiN_x, 2.5 μm i-a-Si:H and 0.2 μm p-a-Si:H layers were deposited continuously. Both SiN_x and a-Si:H layers were deposited by the capacitively coupled rf glow discharge technique. Finally, Al was evaporated and formed.

4. Experimental Results

Characteristics measurements for the TFT and the photodiode were performed using test elements, which are fabricated on the same substrate for this sensor.

Figure 6 shows I_D-V_G characteristics for a-Si:H TFT. Typical TFT on resistance is 400-500 kΩ at V_G =30 V. Mobility and threshold voltage for TFT obtained from V_G -$\sqrt{I_D}$ characteristics are 0.6 $cm^2/V\cdot sec$ and 6~7 V, respectively. On/Off ratio is 10^5 or more. Photo-current for a photodiode under 100 lx (550 nm) exposure is 9×10^{-10}A in over 3 V saturation voltage. Dark current is less than 10^{-13}A at 0 to 15 V. Photoresponse time for the photodiode is less than 0.1 msec. Therefore, high speed image processing is possible. The storage capacitor in the photodiode is 10~20 pF. Then, from Eq.(3), the time constant for photodiode and TFT pair is expected to be 4~10 μsec.

Figure 7 shows the charge transfer characteristics from photosensor to Ci. Ci is 330 pF and T_A is 2.5 μsec. In this case, the time constant for the analog numtiplexer is apploximately 0.2 μsec. Charge transfer time is 20 μsec at V_G =20 V and 5 μsec at V_G=30 V. Ca is estimated at 10 pF, from Eq.(3) and Fig.7. Therefore, afterimage is less than 3 percent. These results agree with estimation from the test elements.

The output wave forms for integrator and voltage developed across C_3 at 4 lx·sec exposure (550 nm) and in the dark are shown in Fig.8. T_G is 20 μsec and T_A is 2.5 μsec. The interval between ϕ_{Ai} and ϕ_{Ai+1} is integrator reset time. In this

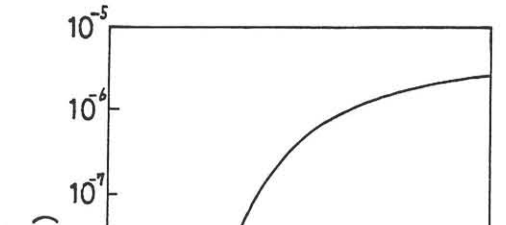

Fig.6 a-Si:H TFT I_D -V_G characteristics case, operation speed is 10 μsec/bit. A large feedthrough, which is due to capacitive coupling of interrogating pulse, appears across C_3 . In general, such a noise is cancelled when the interrogating pulse is off. Nevertheless, an uncancelled value exists which causes a reduction in signal to noise ratio. This uncancelled value is considered due to trapped electrons, which will be released from the traps in the a-Si:H TFT, and the analog multiplexer feedthrough. This noise will be reduced by miniturization of TFT and using the noise reduction method[3]. Integrator output wave form indicates that charge read out from C_3 is completed within 1 μsec. The read out time per bit can be reduced by increasing the number of elements which are switched at one time, as mentioned above. When T_G is 10 μsec and T_A is 1 μsec, operation speed coresponds to 1.3 μsec/bit in a practical 32 bit/column. This speed satisfies the GⅢ mode facsimile requirement.

5. Conclusion

An a-Si:H linear image sensor operated by a-Si:H TFT array has been proposed. In this sensor, a photodiode, which has short photoresponse time, and a high mobility TFT are used to increase operation speed. The photodiode and TFT pair shows 5 μsec read out time at 30 V gate applied voltage. Moreover, effective read out time is greatly reduced by using a novel driving method. Experimental results indicate that operation speed for this sensor is high enough for use in practical facsimile equipment.

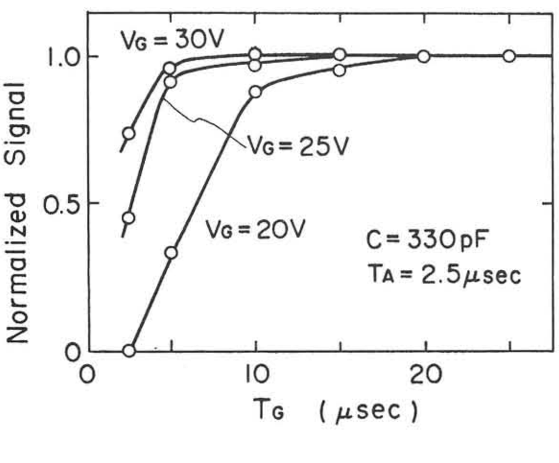

Fig.7 Charge transfer characteristics

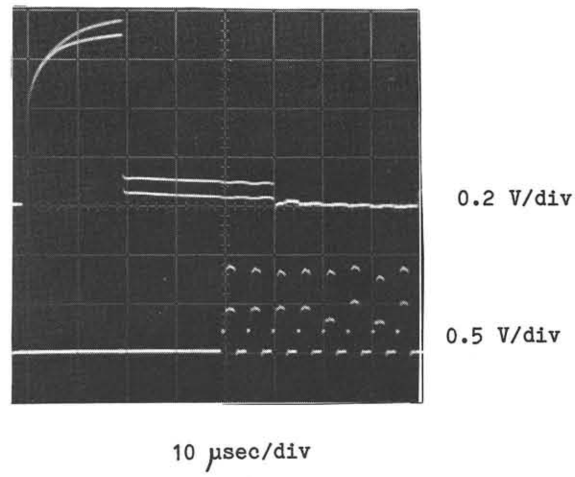

Fig.8 Output wave forms
Upper wave form is transient response of TFT (voltage developed across C_3) and lower wave form is integrator output at 4 lx·sec exposure and in the dark

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