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Reproducible Preparation of Cubic-SiC Single Crystals by Chemical Vapor Deposition

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A single crystal of cubic SiC was reproducibly grown by chemical vapor deposition (CVD) using an SiH_4-C_3H_8-H_2 system on a silicon substrate. To reduce the large lattice mismatch between cubic SiC and silicon, a buffer layer was made by carbonizing the Si substrate in the CVD system. The grown layer was confirmed as a single crystal by examining with reflection electron diffraction and X-ray diffraction. Electrical properties of the epitaxial layer were measured. The mobilities on the (111) plane were larger than those on the (100) plane. The maximum values of the mobility at the present work are 600 $cm^2/V \cdot sec$ for electrons($n=2\times10^{17}$ cm^{-3}) and 650 $cm^2/V \cdot sec$ for holes($p=2\times10^{16}$), respectively. Diode characteristics of pn junctions are also investigated.

1. Introduction

Silicon carbide(SiC) is expected as a material for electronic and optical devices under high temperature and high radiation condition because of its temperature stability and large energy gap. Cubic SiC(one of various polytypes) is attractive owing to the high electron mobility(1000 $cm^2/V \cdot sec$) and the high saturation drift velocity(2.7×10^7 cm/sec at 2×10^5 V/cm)[1,2]. However, crystals of cubic SiC obtained by sublimation process(Lely method)[3] have small sizes and irregular shapes, which has prevented the material from electronic application. Heteroepitaxial growth of SiC on foreign substrates will solve the above problem. Recently, we could obtain rather thick and large-area epitaxial layers of cubic SiC on Si substrates by CVD method with the aid of a buffer layer to release the large lattice mismatch of about 20 %[4,5]. We previously reported the preparation of cubic SiC on Si substrates with a sputtered SiC intermediate layer[6]. In this work, an intermediate buffer layer was grown in the CVD system and details of reproducible single crystal growth are described together with electrical properties.

2. Experimental

The deposition of cubic SiC by pyrolysis of silane(SiH_4) and thermal decomposition of propane (C_3H_8) in a hydrogen flow system was carried out using a horizontal reaction tube with a water-cooled jacket. The reaction tube of 30 mm ID and 440 mm length was made of clear fused quartz. The apparatus used in this experiment has already been reported [6]. After being soaked in HF solution and rinsed in deionized water and aceton, the Si substrate was put on a SiC-coated graphite susceptor ($24\times30\times5$ mm^3). The size of the Si substrate was 10×15 mm^2. The linear velocity(defined as the ratio of the carrier gas flow rate to the cross section of the reaction tube) of the system was approximately 2 cm/sec. The temperature was measured by observing the Si substrate through the water-cooled wall of the reaction tube with an optical pyrometer. The measured temperature was calibrated taking account of the emissivity of Si, but no correction was made for absorption by the water-cooled wall. The entire system was evacuated by a rotary pump and back-filled with H_2. After H_2 flowing for 10 minutes, the Si substrate was heated externally by an rf generator and kept at 1360 °C for 30 minutes. Single crystal growth of cubic SiC layers on Si consists of three distinct processes: etching, carbonization and crystal growth. During each of the processes the H_2 carrier gas flow was maintained at 1000 cc/min. Three processes are as follows.

Process(1): *Etching.*

Before subsequent processes, the Si substrate is etched by heating to 1000 °C in a HCl (10 cc/min) flow for 5 minutes. After HCl flow is shutt off,

the H_2 flow is kept for 5 minutes at a substrate temperature of 800 °C to flush the residual HCl gas and then the substrate temperature is returned to near room temperature.

Process(2): *Buffer layer formation.*

This process provides the buffer layer necessary to obtain good SiC growth on the Si substrate by carbonization. A flow of C_3H_8 (1.2 cc/min) is introduced into the reaction tube just before heating the substrate. Then the substrate temperature is raised quickly to 1360 °C for 2 minutes and the C_3H_8 flow is shutt off and the substrate temperature is lowered to 1330 °C. To flush off the residual C_3H_8 gas from the reaction tube, the H_2 flow is kept for 5 minutes. An optimum carbonization time and temperature program of this process were determined by various experiments, which are described later.

Process(3): *Crystal growth.*

The deposition of cubic SiC is carried out at a substrate temperature of 1330 °C with the standard gas composition: $H_2 \sim 1000$ cc/min, $SiH_4 \sim 0.3$ cc/min and $C_3H_8 \sim 0.12$ cc/min. The deposition time was usually 30 minutes. Under these conditions, a cubic SiC single crystal layer can be grown on the buffer layer. When the desired growth time has been achieved, the SiH_4 and C_3H_8 flows are shutt off. The reaction tube was flushed with H_2 and then the substrate temperature is returned to room temperature. When the p-type epitaxial layer is needed, diborane(B_2H_6) is added to the reaction gases of process(3). The temperature program of the crystal growth is shown in Fig.1.

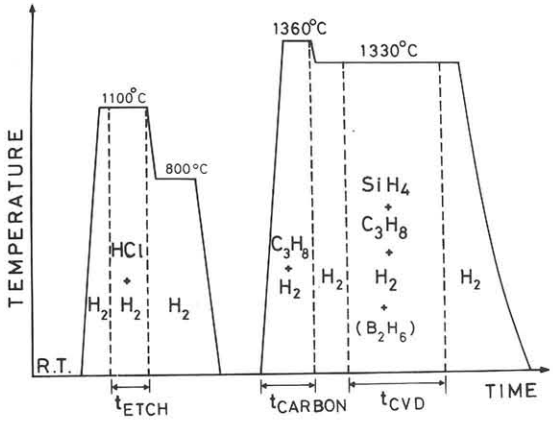


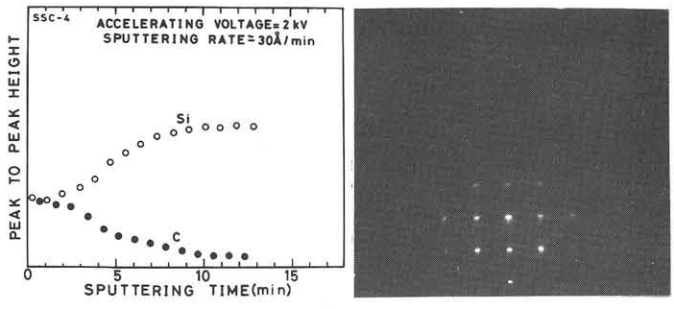
Fig.1 Temperature program of the crystal growth.

The thickness of the grown cubic SiC layer was measured by interference pattern from the reflectivity of the grown layer in the visible light region. The surface morphology of the grown layer was observed by scanning electron microscope (SEM). To study the crystallinity of the cubic SiC layers, the layers were examined by reflection electron diffraction(RED) and X-ray diffraction methods. Electrical properties were measured by van der Pauw's method.

3. Result and discussion

Buffer layer

Buffer layer formation is very sensitive to preparation condition like a temperature program. Before the substrate temperature rise, the reaction tube must be saturated with C_cH_8 gas. Carbonization temperature is at around 1360 °C. The higher the substrate temperature, the better the buffer layer is. Carbonization time is also a key parameter and the optimum condition is found to be about 2 minutes. If it is longer than 2 minutes, the crystallinity of the subsequent grown layer on the buffer layer becomes bad. The depth profile of the buffer layer was analyzed by Auger electron spectroscopy (AES) as shown in Fig.2. In AES analysis. bulk SiC made by Lely method was used as a standard sample having exact stoichiometry of SiC.



(a) (b)

Fig.2 (a) AES depth profile of the buffer layer prepared by 2 minutes-carbonization. (b) RED pattern of the buffer layer.

The atomic ratio of the buffer layer was determined by comparing the Auger signals (peak height of Si_{LVV} and C_{KLL}) of the buffer layer and those from the standard sample. The thickness of the buffer layer was approximately 300 Å. The top surface (80 Å) of the buffer layer had stoichiometry (Si/C=1) of SiC, but the buffer layer of

about 220 Å thickness left behind had a compositional change from stoichiometry of SiC to Si. We tentatively call this top surface having stoichiometry of SiC as the *first SiC layer* for subsequent epitaxial growth. The RED pattern of the buffer layer shown in Fig.1(b) indicates a single crystalline feature. When the carbonization time was kept at about 10 minutes, the *first SiC layer* became a thickness of about 130 Å, but the RED pattern from this buffer layer contained faint rings together with spots. The buffer layer was also characterized by X-ray rocking curve measurements for the CVD grown layer on it. In this case, carbonization time was changed from 2 to 15 minutes keeping the subsequent crystal growth condition constant. The grown layer on the buffer layer prepared with 2 minutes-carbonization showed the narrowest half width in X-ray rocking curve, indicating good crystallinity. The most interesting aspect of our observation on the buffer layer is the fact that the epitaxial layer was not grown on the buffer layer carbonized for longer than 10 minutes. This phenomenon seems to relate to the thickness of the *first SiC layer*. The thicker *first SiC layer* might increase the stress between cubic SiC and Si. Consequently, the compositionally mixed layer could not release this stress and the RED pattern from the buffer layer showed faint rings, indicating a polycrystalline feature. We believe that there is an optimum thickness of the *first SiC layer* and the compositionally mixed layer for better epitaxial growth of cubic SiC.

Crystal growth

Single crystals of cubic SiC were grown on the Si substrate under the standard condition mentioned in process(3). The relation between the thickness of the grown layer and the growth time was studied. The thickness was approximately proportional to the growth time . The growth rate was about 600 Å/min. The growth rate did not depend on the orientation of the substrate.

The crystallinity of the grown layer was examined by X-ray diffraction with a copper target. Let θ is Bragg angle. A strong peak appeared at $2\theta=41.40^{\circ}$ for the layer grown on the (100) substrate. A strong peak also appeared at $2\theta=36.65^{\circ}$ for the layer grown on the (111) substrate. The grown layers were also examined by RED, and every RED pattern showed streaky spot pattern which was indexed as cubic SiC. These evidences indicate that cubic SiC is epitaxially grown on the Si substrate.

The surface was smooth and mirror like for undoped- and B_2H_6-doped grown layers with 1μm thick. When B_2H_6 flow rate of 5×10^{-3} cc/min was added to the main stream with the standard condition, the grown layer with p-type conduction was obtained.

Electrical properties

An undoped cubic SiC layer was grown on p-type Si (ρ=10-20 Ωcm) and a p-type SiC layer was grown on n-Si (ρ=10-20 Ωcm). Owing to heterojunction properties of cubic SiC and Si, the depletion layer was thought to separate electrical conduction of the grown layer from the substrate. Four ohmic contacts were made at the edges of the crystal by evaporating gold-tantalum alloy for n-type grown layer and aluminium-silicon alloy for the p-type grown layer. Gold wires were attached to the contacts with silver paste and the crystal was mounted on an insulating holder. The measured values of the electron mobility and the carrier concentration versus the thickness of the grown layer are shown in Fig.3.

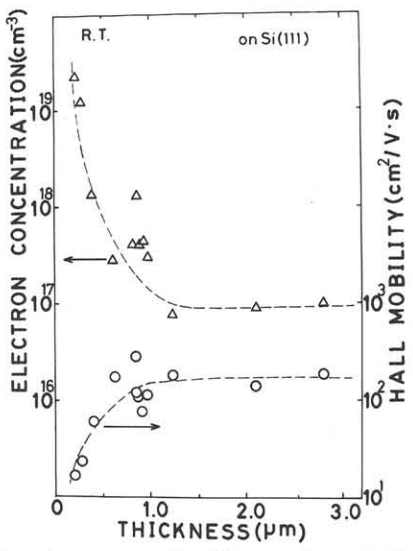


Fig.3 Carrier concentration and mobility versus thickness of the grown layer on the (111) plane: measured at room temperature.

The undoped layer always showed n-type conduction. As the thickness increases up to 1 μm, the electron concentration of the grown layer on the (111) plane decreases, then reaches to a constant value ($n=1\times10^{17}$ cm^{-3}). The electron mobility of the grown

layer on the (111) plane increases as the thickness increases. The buffer layer showed always n-type conduction confirmed by thermo-probe method, so it seems to have a role of an donor-like. On the grown layer on the (111) plane, this donor like nature dominantly appeared and resulting the higher electron concentration at the interface. On the other hand, on the (100) plane, the electron concentration increased up to 1 μm and reached constant value. Thus electrical properties are strongly influenced on the orientation of the substrate.

In summarizing the electrical properties, the Hall mobility versus the carrier concentration for n- and p-type grown layers are shown in Fig.4.

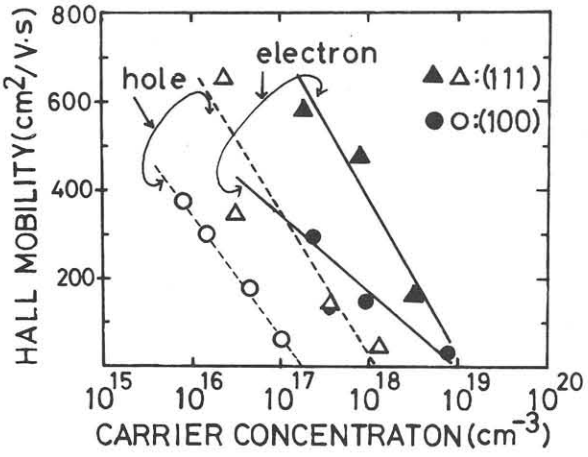


Fig.4 Hall mobility versus carrier concentration for n-type and p-type grown layer.

As the carrier concentration of the grown layer increases the Hall mobilities of electrons and holes decrease. The mobilities on the (111) plane are larger than those on the (100) plane. The maximum values at the present work are 600 $cm^2/V\cdot s$ for electrons($n=2\times10^{17}$ cm^{-3}) and 650 $cm^2/V\cdot s$ for holes($p=2\times10^{16}$ cm^{-3}), respectively.

Pn junctions were epitaxially grown on Si substrates by changing the reaction gases to get the different conduction type. Mesa diodes of 2x2 mm^2 were made from these epitaxial layers by masking and etching techniques. Diode structures were n-SiC/p-SiC/p^+-Si and p-SiC/n-SiC/n^+-Si. Current-voltage(I-V) and capacitance-voltage(C-V) characteristics of the diodes were measured at room temperature. The I-V characteristics of the diode, which is shown in Fig.5, obeyed the relation of $I\propto\exp(eV/nkT)$ with n=2.5-4. The diffusion voltage was about 1.3 V. The C-V curve had the relation of $1/C^2\propto V$, which implies an abrupt junction. The temperature dependence of the diode characteristics was also investigated.

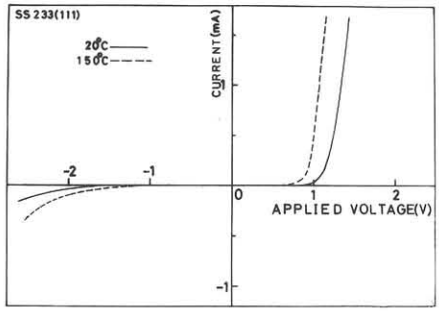


Fig.5 Current-voltage characteristics of the diode measured at 20°C and 150 °C.

The building voltage was changed from 1.25 to 1V when the temperature was risen from 20 °C to 150°C. The leakage current at a reverse voltage of 2 V changed from 45 μA to 90 μA with a temperature-rise. A rectification ratio at 1 V measured at 150 °C was about 100, showing good rectifying characeristics.

4. Conclusion

Single crystals of cubic SiC were obtained reproducibl1y by CVD at a substrate temperature of 1330 °C on Si substrates by using buffer layers prepared in the CVD system. A key point of the buffer layer was elucidated the thickness of the *first SiC layer* should be 80 Å and the total thickness of the buffer layer shoud be about 300 Å. The grown layer showed almost a mirror surface. Electrical properties of the grown layer for n- and p-types were studied. The electron concentration near the interface between cubic SiC and Si was strongly influenced by the orientation of the substrates. The Hall mobilities versus the carrier concentrations were investigated and the maximum mobilities were 600 $cm^2/V\cdot s$ for electrons($n=2\times10^{17}$ cm^{-3}) and 650 $cm^2/V\cdot s$ for holes($p=2\times10^{16}$ cm^{-3}), respectively. Pn junctions were made by CVD and those characteristics were measured.

Acknowledgements

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