FABRICATION OF SUBMICRON SEMICONDUCTOR DEVICES BY HOLOGRAPHIC METHOD --- IV SUBMICRON GATE PROCESS

N. NOMURA, Y. HIROFUJI, T. EDAMATSU and K. KUGIMIYA
Central Research Lab., Matsushita Electric Industrial Co., Ltd.

Holographic photolithography has been shown to have a high throughput in a submicron pattern formation.[1] Submicron resist patterns with a high aspect ratio were obtained by the three layered resist structure in combination with holographic photolithography.[1] A high precision alignment was realized by a new holographic configuration which utilized the interference between a grating on a substrate and a fringe of two beams in a space.[2] In this paper, we describe a holographic submicron gate process and show characteristics of n-channel MOSFETs fabricated by the holographic process.

The holographic submicron gate process was similar to a conventional n-channel MOS process except the holographic gate formation. Fig.1 illustrates the essential process steps of gate fabrication. After deposition of 0.16 μm thick poly-Si on a 20 nm thick gate oxide, three layered resist structure was formed (upper AZ resist 0.35 μm/Si_3N_4 0.1 μm/AZ resist 1 μm). 1 μm gate resist patterns were formed by a conventional U.V. radiation and development. The developed upper resist was again exposed to holographic fringes (0.5 μm L/S). By the secondary development, 1 μm gate resist patterns were made narrower to 0.5 μm. Wide electrode areas were also exposed to holographic fringes but remained unchanged (Fig.2). The 0.5 μm gate patterns were reprecated to the Si_3N_4 film and further to the 1 μm thick AZ resist by reactive ion etching. Gate resist patterns with a high aspect ratio (1 μm thick/0.5 μm wide) were thus realized as shown in Fig.2.

Source/drains were formed by a self-aligning technique as a conventional process. The final junction depth of less than 0.15 μm, as required by scaling considerations, was achieved by a high dose, low energy single implantation (As^+ 2×10^{15} cm^{-2} at 25 keV) and double implantation (As^+ 2×10^{15} cm^{-2} at 25 keV/P^+ 1×10^{14} cm^{-2} at 30 keV) followed by annealing at 900°C for 20 min. Fig.3 shows simulated impurity profiles. The final profile for single As^+ implantation showed a calculated junction depth of 900 Å and for double As^+/P^+ implantation, 1300 Å. The channel B^+ concentration was 9×10^{16} cm^{-3} in the 1 Ωcm P-type (1 0 0) wafer and V_{th}, approximately 0.5 Volt.

Fig.4 shows V-I characteristics in ohmic and saturation ranges of a device with an observed gate pattern length of 0.45 μm and a double As^+/P^+ source/drain implantation. At a gate voltage of 5 Volt and without substrate bias, the breakdown of the drain junction occured at about 4.6 Volt

for a device with a double implantation and at about 4.1 Volt for a device with a single implantation. The improvement was about 0.5 Volt by a double implantation graded junction.

We have demonstrated that the holographic photolithography is one of the practical methods to fabricate a submicron MOSFET structure with a high precision alignment and a high throughput. By the holographic method, even shorter gate length, 600 Å, can be realized using an eximer laser, 2300 Å.

References
1) N. Nomura et al. Inst. Elect. Comm. Engr. Jpn. SSD82-186.
2) N. Nomura et al. to be published.

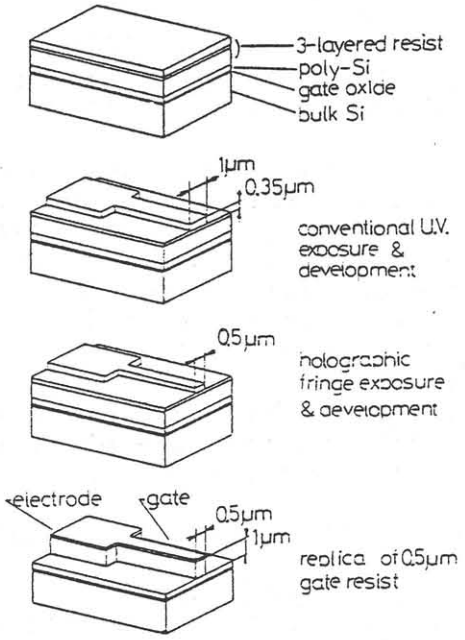

Fig.1 Illustration of holographic submicron gate process.

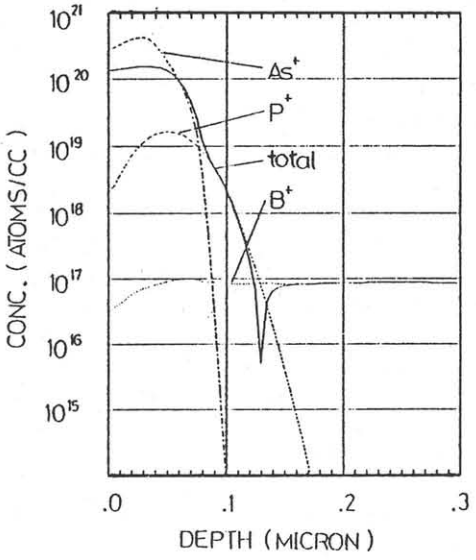

Fig.3 Impurity profiles of simulated concentration in the source/drain areas.

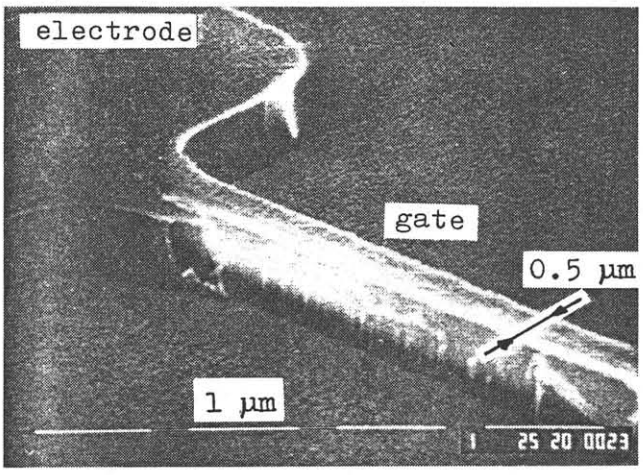

Fig.2 SEM view of a 0.5 μm gate pattern.

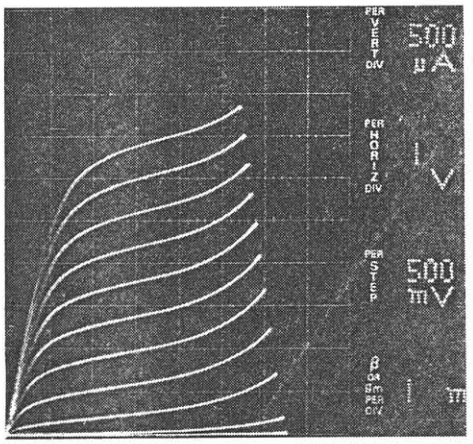

Fig.4 Current-voltage characteristics with zero substrate bias and 5 V maximum on the gate. T_{ox}=20nm, L=.45μm, W=20μm.