Induced Dislocations and Change of the EL2 Trap Density in Undoped Bulk GaAs by Si_3N_4 or SiO_2 Cap Annealing

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Undoped semi-insulating LEC GaAs is thought to be the key material for GaAs Integrated Circuits. However, there are still problems in uniformity and reproducibility of FETs fabricated by the direct ion implantation[1]. Distributions of dislocations and deep electron trap EL2 in a wafer might be responsible for these nonuniformities[2,3]. In practical applications for GaAs ICs, the ion-implanted GaAs wafers must be heat treated at 800°C or 850°C with Si_3N_4 capping or in arsenic atmosphere.

In this paper, we show that many dislocations are induced during the annealing process with Si_3N_4 capping at 700°C -850°C when thickness of Si_3N_4 is more than 2000Å, and that the surface EL2 density decreases for LEC GaAs even when the surface is capped with Si_3N_4, whereas for HB GaAs, change of the EL2 density can be prevented by capping with Si_3N_4, SiO_2 or GaAs.

GaAs substrates used in this study were undoped conductive LEC and HB GaAs obtained from big GaAs suppliers in Japan. Si_3N_4 and SiO_2 were deposited by ANELVA plasma CVD system (PED 301) at 250°C and 300°C, respectively. The deposition rate was about 400Å per minute. The EL2 density was measured by a normal DLTS method and calculated by taking into account the non-ionized front region of the depletion layer[4].

Figure 1 shows profiles of the EL2 densities in LEC and HB GaAs which were heat treated at 700°C for 1 hour in a hydrogen atmosphere. The EL2 density at the surface is decreased nearly two orders of magnitudes for LEC GaAs and to a half of the original value for HB GaAs. Decrease of the EL2 density is thought to be due to arsenic evaporation[5]. In order to see effect of capping and atmosphere, LEC and HB GaAs were heat treated with Si_3N_4, SiO_2 capping or by covering with another GaAs wafer in a hydrogen atmosphere. The results are shown in Fig.2 and Table 1. A large difference of the EL2 change is observed between LEC and HB GaAs. The decrease of the EL2 density in HB GaAs can be prevented by Si_3N_4 or SiO_2 capping, or GaAs covering, whereas for LEC GaAs, the EL2 density decreases always even when the surface is capped with Si_3N_4 or SiO_2[5]. This fact means that the EL2 in LEC and HB GaAs has different properties even though activation energies and emission rates are almost the same. To see the effect of hydrogen,[6] some samples were heat treated in vacuum. Decrease of the EL2 density was the largest in these samples. It means that the arsenic loss is primary reason of the decrease of the EL2 density,even though the decrease of EL2 in capped LEC GaAs can not be understood well in that case.

Another thing to be noted is that some HB samples capped by Si_3N_4 show a higher EL2 density than that of as grown samples. In such samples, some scratches were seen on step etched surfaces. In order to see induced defects, samples capped by Si_3N_4 with different thickness were heat treated at 700°C, 750°C, 800°C and 850°C, and were etched by molten KOH. Many scratches were seen on the samples capped by Si_3N_4 whose thickness is more than 2000Å as shown in Fig.3(a). The scratches were revealed to be clusters of dislocations as shown in Fig.3(b). The increased EL2 density might

be due to these induced dislocations[7].

No induced dislocations was observed on samples capped by SiO_2 with 6000Å and Si_3N_4 with less than 1000Å.

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References

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Table 1, Change of EL2 density by heat treatments

cap \ (cm^{-3})		HB $x10^{16}$	LEC $x10^{16}$
as grown		1.3	3.0
700°C, 1hr	H_2	0.2	0.1
	Si_3N_4/H_2	3.9	0.05
	SiO_2/H_2	1.3	0.17
	GaAs/H_2	1.4	1.2
	vacuum	0.04	---
800°C, 1 hr	Si_3N_4/H_2	0.48	---
	SiO_2/H_2	1.8	---

--- : semi-insulating

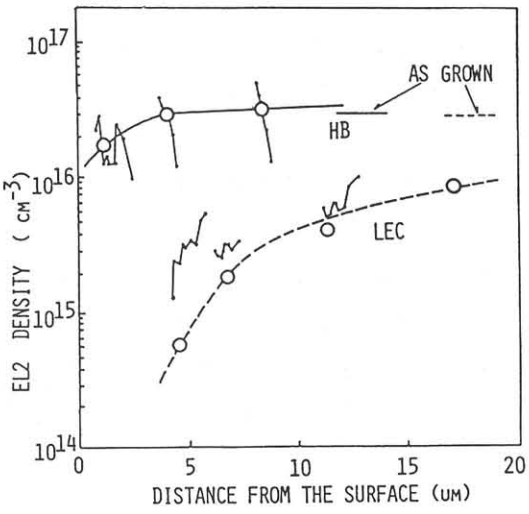

Fig.1, The EL2 density profiles of LEC and HB GaAs heat treated at 700°C for 1 hour in a hydrogen atmosphere.

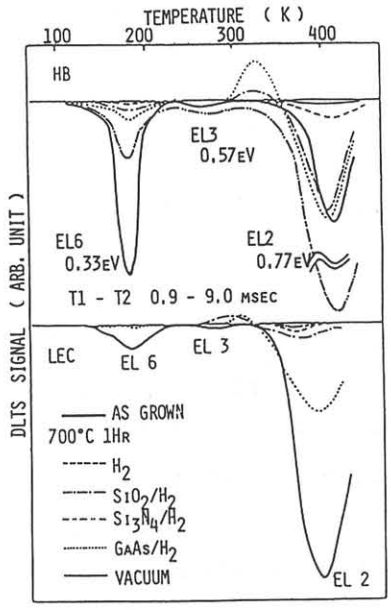

Fig.2, DLTS signals for LEC and HB GaAs heat treated with various capping.

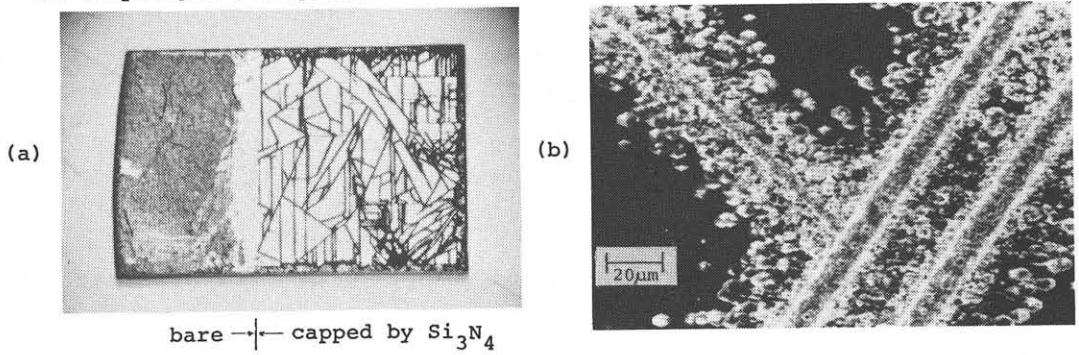

Fig.3, Scratches (a) and etch pits (b) on a GaAs wafer which was heat treated at 850°C for 30 minutes with 2000Å Si_3N_4 capping. Etch pits were revealed by molten KOH. The wafer is (100) oriented.