METAL/Al_2O_3/InP MISFET RING OSCILLATOR

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InP MISFET is a very promising high speed device for post Si VLSIs because of the high electron velocity in InP and the availability of semi-insulating substrates. Although InP MISFET has various potential advantages over GaAs MESFET such as wide dynamic range due to the insulating nature of the gate, InP MISFET logics have not yet been fully investigated.

In this paper, in order to demonstrate the potential of InP MISFET as well as the capability of the process employed, a preliminary result on the fabrication and the operation of InP MISFET ring oscillators is reported.

Five stage ring oscillators have been fabricated using enhancement/depletion(E/D) type inverters. The process starts with ion-implantation of Si into Fe-doped semi-insulating InP substrates at 300keV with a dose of $1x10^{14}/cm^2$ followed by annealing at 750 °C for 20 min with PSG encapsulation to form surface n^+ layers. After forming mesas for isolation, Au-Ge ohmic contacts are formed for source and drain contacts. The implanted layer at the channel regions of the E/D FETs is separately thinned to control the threshold voltage(V_T) of each

type of FETs. The V_T of FETs can be controlled by monitoring the channel conductance. Al film is then deposited in vacuum onto the wafer. Al film on the channel regions is selectively anodized to form Al_2O_3 gate insulator. The electrolyte used in anodization is AGW, which is a mixture of 3% aqueous solution of tartaric acid and propylen glycol in ratio of 1:9. The thickness of the gate insulator is 1200Å. Finally, evaporation and lift-off are done to form an Al gate electrode. The gate length of E-FET is 5μm and 20μm for D-FET and the gate width is 200μm for E- and D-FETs.

The fastest ring oscillator showed propagation delay per gate t_{pd}=25ns with power delay product P t_{pd}=800fJ at supply voltage V_{DD}=1V at room temperature. At -78 ℃ the propagation delay was 7ns and associated P t_{pd}=600fJ at V_{DD}=1V. The propagation delay is believed to be limited by the large input capacitance of the inverter due to wide gate width of 200μm. The difference between the two temperatures may be the result of the change in drift characteristic.

Although the propagation delay and the power delay product are limited by the non-optimized dimension of the devices in the ring oscillator, scaling this result to the reduced gate length and width together with the employment of double layer gate insulator structure, which is known to give higher effective mobility and lower drain current drift, should result in great improvement of performance.