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Ultra Sharp Trench Capacitors Formed by Peripheral Etching

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Peripheral etching technique has been applied for forming trench capacitors. Ultra sharp trenches with a width of a quarter micron and a depth of 3 um were completely filled with SiO_2 and poly Si. The oxide breakdown strength, oxide leakage current and n^+p junction leakage current are acceptable to design requirements of megabit level d-RAMs. This technique offers advantages over conventional trench capacitors.

I INTRODUCTION

In high density d-RAMs beyond 1 Mbit, cell storage capacitance is one of the most important design parameters. When cell size reduced to obtain high density, the cell storage capacitance must remain high enough for soft error immunity. Trench capacitor or corrugated capacitor cells have received considerable attention from this point of view for 1 to 4 Mbit d-RAMs (1) (2). Since these trench capacitors are conventionally formed in Si substrates by RIE or other dry etching, the trench width is transferred from resist mask pattern having still a large size. A new etching technique which can form very sharp trenches less than 0.25 um wide has been developed.

This paper describes the peripheral etching technique to produce ultra sharp trenches without any restriction on the resist pattern or any sophisticated processes. The characteristics of the ultra sharp trench capacitors are also presented.

II PERIPHERAL ETCHING TECHNIQUE

For forming ultra sharp trench capacitors the key technology is peripheral etching (P-Etch) which entails selective etching of materials only at the periphery of the resist pattern. The possibility of selective etching at the periphery of the resist pattern was found in the reactive ion etching process for molybdenum silicide ($MoSi_2$) film (3). A $MoSi_2$ film has superior anti-chemical properties and is applicable to existing VLSI production processes.

The etch rates of $MoSi_2$, resist (AZ-1350J) and SiO_2 films in the experiments are shown in Fig. 1. The P-Etch for $MoSi_2$/resist layers occurs under a reactive etching gas of CCl_4 mixed with O_2 ranging from 60 to 70 %. In this range, since most of the O_2 gas is consumed in oxidizing $MoSi_2$ films and reducing resist films to ash, O_2 gas beneath the edge of the resist pattern is short locally, resulting in etching the $MoSi_2$ film at the periphery of the resist mask. This process produces very fine and steep grooves on the $MoSi_2$ film in spite of the width of the resist mask. Figure 2 shows $MoSi_2$ film peripheral etching width as a function of etching time.

III FABRICATION PROCESS

The process flow for fabrication of samples is shown in Fig. 3. A field oxide is formed by using the conventional local oxidation process, and then a $MoSi_2$ film is deposited by DC magnetron sputtering. A spin-coated resist film is patterned as the resist mask edge coincides with locations whose trench capacitors are to be

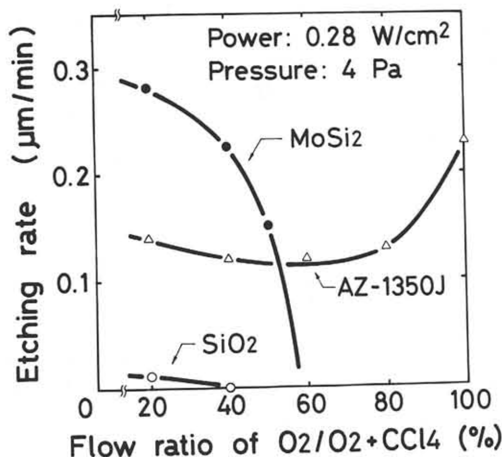

Fig.1. Etching rates of $MoSi_2$, SiO_2 and AZ-1350J as a function of flow ratio of $O_2/O_2 + CCl_4$

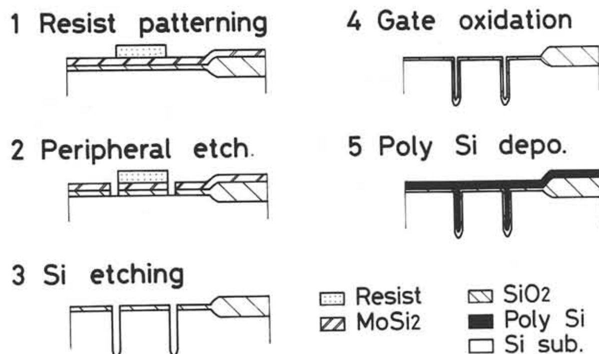

Fig.3. Process flow for ultra sharp trench capacitors by P-Etch

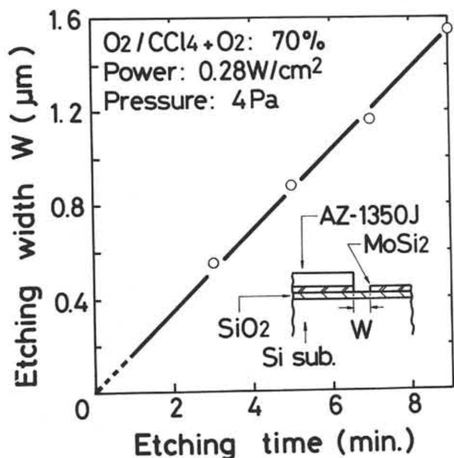

Fig.2. $MoSi_2$ film peripheral etching width as a function of etching time

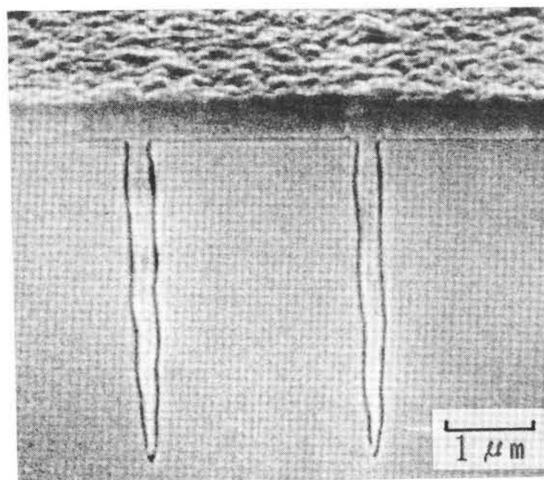

Fig.4. Cross section of ultra sharp trench capacitors filled with thermal SiO_2 and poly Si

formed. In the RIE condition mentioned above, P-Etch is done for the $MoSi_2$ film. The pattern of the $MoSi_2$ film is used as the etching mask for the silicon substrates. To form ultra sharp trench capacitors, the Si substrate is etched by conventional RIE. Trenches with a depth of 3 um and a width of 0.2 um are formed. Then, the trench is completely filled with thermal SiO_2 and poly Si as shown in Fig. 4.

IV TRENCH CAPACITOR CHARACTERISTICS

(1) Junction leakage current

Low leakage current of a pn junction formed just below a trench capacitor is one of the design requirements for d-RAMs. The n^+p junction were fabricated to test the leakage current caused by residue and contamination in the trench. The n^+p junction, surrounded by a 3 um deep trench filled with SiO_2 and poly Si, was formed by As^+ ion implantation and annealing.

Figure 5 shows reverse current of the junction with an area of 1.27×10^5 um^2. Although the leakage level is slightly higher than that of a conventional junction surrounded with recessed SiO_2 produced by selective oxidation, the level is acceptable for production of d-RAMs.

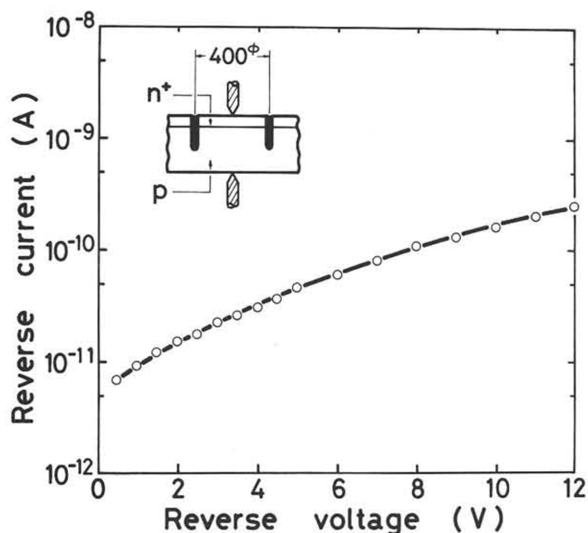

Fig.5. Reverse current of a junction surrounded with a 3 um deep trench

(2) Dielectric breakdown

Breakdown voltage histograms of both ultra sharp trench and conventional plane capacitors were measured by using the same gate pattern of poly Si. The test trench capacitor includes plenty of trenches with 3 um depth in a gate region as shown in Fig. 6. As seen from Fig. 7, the dielectric strength of the trench capacitor is typically as high as 8 MV/cm for a SiO_2 film with a thickness of 25 nm. The value is a little smaller than that of the plane capacitor. This may be caused by structural effects; localized thinning of SiO_2 at the shoulder of the trench and current-crowding at the same point. The ultra sharp tip of the trench is not likely the origin of breakdown degradation. Degradation of breakdown voltages ranging from 8 to 18 V may be caused by residue and/or contaminants on the surface of the trench. Although these should be removed, the breakdown voltage is fundamentally satisfactory for practical production of d-RAMs.

(3) Oxide leakage

Leakage currents of the same capacitors as those in Fig.6 are shown in Fig.8. The oxide leakage is as low as that of a conventional plane capacitor under gate voltage of 5 V.

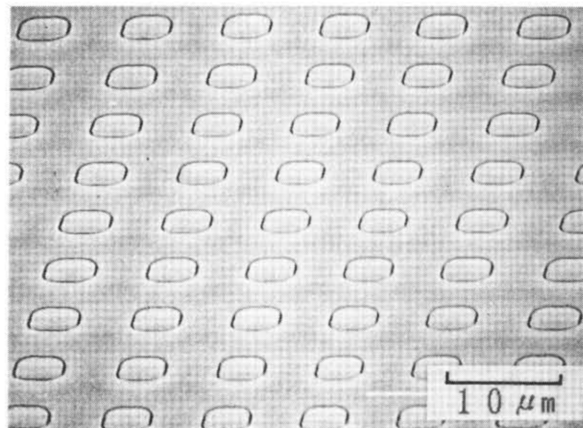

Fig.6. SEM picture of P-etched trenches used for experiment

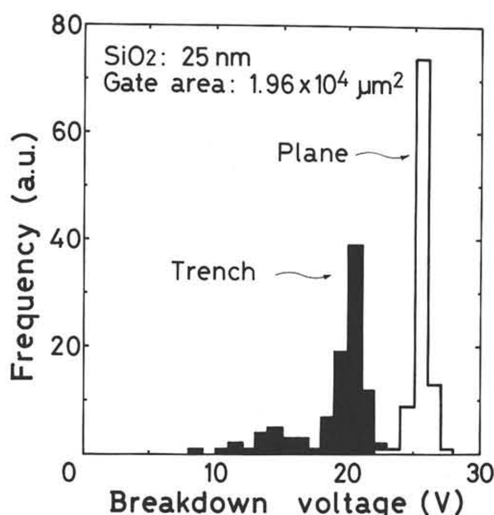

Fig.7. Breakdown voltage histograms for both ultra sharp trench and plane capacitors

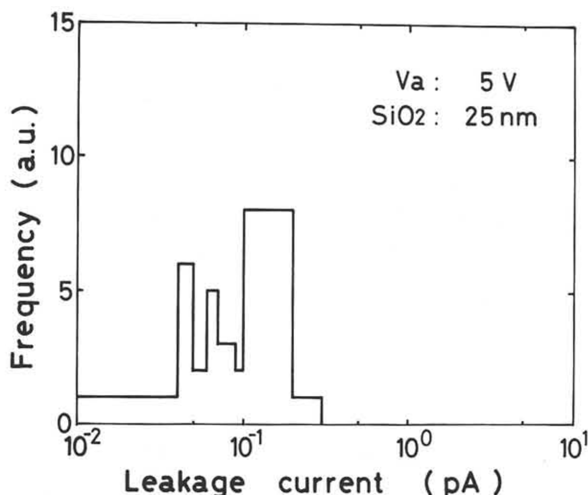

Fig.8. Leakage current histogram for ultra sharp trench capacitors

V CAPACITANCE EVALUATION

Capacitances of the ultra sharp trench capacitors were calculated with respect to design rule and shown in Fig.9. The trench pattern was aligned inside a plane capacitor area. Assuming a trench depth of 3 um, SiO_2 thickness of 20 nm and the design rule of 1 um, the capacitance is 3.7 times that of a conventional plane capacitor formed on the same area, and 50 % larger than that of a capacitor with a conventionally formed trench up to the design rule of about 0.6 um. The minimum design rule, for which the present technique offers a capacitance advantage, is due to the quarter micron trench width.

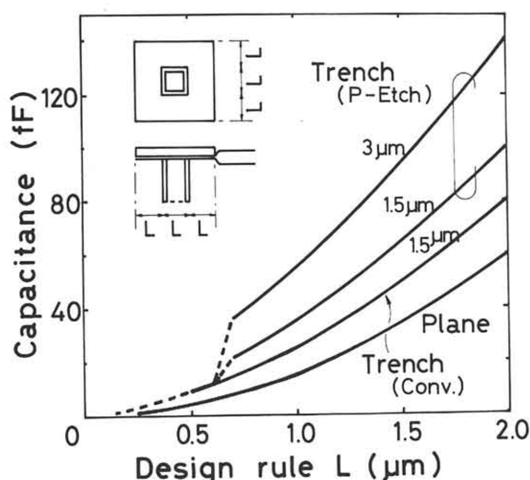

Fig.9. Calculated capacitances with respect to design rule for ultra sharp trench, conventional trench and plane capacitors (SiO_2 thickness ; 20 nm)

VI CONCLUSIONS

Peripheral etching technique has been applied for forming trench capacitors. Ultra sharp trenches with a width of a quarter micron and a depth of 3 um were completely filled with SiO_2 and poly Si. The oxide breakdown strength, oxide leakage current and n^+p junction leakage current are acceptable to design requirements of megabit level d-RAMs. This technique offers advantages over conventional trench capacitors.

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