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Intrinsic Gettering Effects on Reactive Ion Etching Damage and Thin Oxide Film Breakdown

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Two new intrinsic gettering applications are proposed. One is suppression of lifetime degradation by reactive ion etching at a high ion acceleration voltage, where intrinsic gettering efficiently eliminates damage-induced surface defects. The other is improvement in breakdown voltage of thermally grown thin oxide films, which is accomplished by gettering contamination during oxidation. These new applications will be useful tools in developing future VLSIs.

1. Introduction

Since Tan's proposal on intrinsic gettering (IG),[1] a lot of investigations have been performed. IG has succeeded in eliminating the device problems such as p-n junction leakage,[2] area imager crosstalk[3] and dynamic MOS RAM yield loss.[4] It is understood that these IG effects are all attributed to the phenomenon wherein undesirable impurities are swept together by micro-defects in specimen bulk. It has recently been found that the following two problems become essential in submicrometer rule device fabrication: lifetime degradation by reactive ion etching (RIE) damage[5] and reduction in breakdown voltage of thin gate oxide films.[6] The former is possibly caused by the strain left by RIE or a combination of the strain and other defects, while the latter is caused by contamination[7] or substrate surface precipitation.[6] Therefore, the possibility should exist that these problems can be erased by IG application.

In the present paper, we first demonstrate successful IG applications for eliminating these problems and then discuss the possible reason for these IG effects.

2. Experimental

Silicon wafers were sliced from <100> oriented, boron-doped, 4.4 ~ 5.7 Ω·cm CZ as-grown ingots. IG wafers which had denuded zones of about 15 μm in depth and bulk defects from 10^8 to 5×10^{12} cm^{-3} in density were prepared for investigating IG effects on RIE damage. The wafers with and without IG were etched in a contamination-free RIE reactor whose walls were covered by teflon. Ion acceleration voltage (V_a) was varied between 300 and 1000 V, with the ion dose amount kept constant. The RIE etchant was a mixture of CF_4 and H_2.

After RIE was followed by surface cleaning, MOS capacitors were made on the wafers. Each capacitor had a 50 nm-thick oxide film and a 500 μm-diameter aluminum gate electrode with a guard ring. The IG effect was evaluated by minority carrier lifetime measured by the MOS C-t method. Gate aluminum and oxide on the wafers were then removed and the wafer surface was examined by chemical etching combined with optical microscopy. Heavy metal contamination due to RIE was also examined by deep level transient spectroscopy (DLTS) using Schottky diodes on as-RIE'd wafers.

Investigation of the IG effect on breakdown voltage and leakage current of thin oxide films was carried out by the following procedure. Samples were pre-oxidized at 1000 °C in dry oxygen to form 50 nm-thick oxide films. Some of them were annealed at 700 °C for 48 hours in an Ar ambient to introduce bulk defects. All samples were then annealed at 1100 °C for 18 hours in an Ar ambient in a manner similar to the

CMOS well drive-in process. Finally, the MOS capacitors with 15 nm-thick oxide films were fabricated on them, as well as on the control wafers which did not receive the above heat treatment. Oxide breakdown voltage and leakage current were then measured.

3. Results and discussion

3.1 The IG effect on RIE damage

Lifetime in the RIE wafers with and without IG is shown as a function of V_a in Fig. 1. Lifetime in the wafers without IG (ungettered) decreases steadily as V_a increases and decreases abruptly to a few microseconds at V_a = 1000 V. Lifetime degradation does not take place in IG wafers against RIE at the conditions up to V_a = 1000 V.

This decrease in lifetime for ungettered wafers implies degradation of crystal surface quality. High density surface stacking faults of about 1 μm in length were induced by RIE at V_a = 1000 V as depicted in Fig. 2. In order to examine the electrical activity of RIE-induced stacking faults, a relation between lifetime and stacking fault density is additionally plotted in Fig. 3. The lifetime values for uncontaminated stacking faults of approximately 10 μm in length generated from bulk oxide precipitates and those for heavy metal contaminated faults of about 1 μm in length generated by RIE in a reactor with bare stainless walls lie almost on the same degradation curve.[8)]

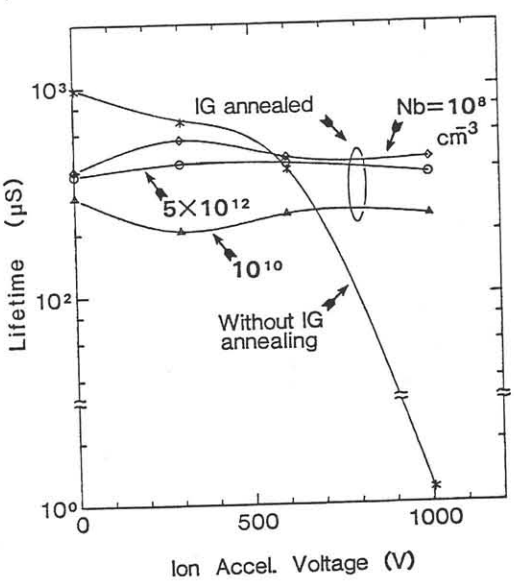

Fig. 1. Intrinsic gettering effect on RIE damage at various ion acceleration voltages for several bulk defect densities.

Since the present result, indicated by the symbol x, lies on the curve, the electrical activity of RIE-induced stacking faults at a high V_a is about ten times stronger than that of uncontaminated faults, considering defect size difference. On the other hand, no defects were observed in the ungettered wafers that were RIE-processed below V_a = 600 V nor in the IG wafers. However, a slight dependence of lifetime in the ungettered wafers on a V_a less than 600 V, as shown in Fig. 1, suggests that some kinds of micro-defects that are electrically less active than the stacking faults may exist in the surface of ungettered wafers.

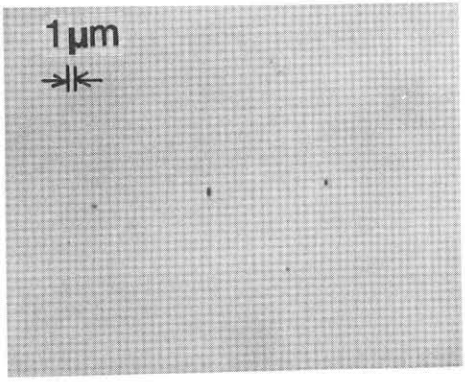

Fig. 2. A microphotograph of surface stacking faults induced by RIE at V_a=1000 V.

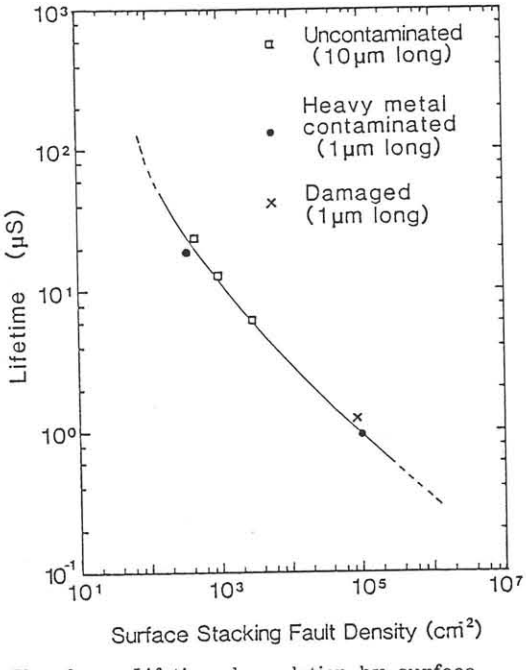

Fig. 3. Lifetime degradation by surface stacking faults generated by bulk precipitates, heavy metal contamination and RIE damage.

Possible nucleation sites of RIE-induced stacking faults are damage, heavy metal contamination or carbon. Heavy metals such as nickel, chromium or iron were not detected by DLTS, suggesting that they are not responsible in this case. Although it is not clear whether damage (structural defects) or carbon is responsible, most carbon atoms on the substrates were removed during cleaning. Moreover, it is suggested that the diffusion coefficient of carbon seems too slow to be gettered by the bulk defects (extraordinary fast diffusion takes place only at high carbon concentration). Surface damage induces stacking faults via two mechanisms, that is, the damage provides nucleation sites and constituents (intrinsic point defects) and release of strain and stress or absorption of intrinsic point defects emitted from a damaged layer might take place in IG wafers, resulting in suppression of surface defect generation (see Fig. 4). Unobservable defects induced at a low V_a might be suppressed by such a similar mechanism.

3.2 The IG effect on thin oxide films

Two IG effects were observed: (1) Reduction in gate leakage current in the low electric field (less than 7 MV/cm), with typical current-voltage characteristics of the oxide films shown in Fig. 5. As shown, the leakage current in ungettered wafers, subjected to high temperature annealing, is several times higher than that in the control wafers, but is reduced by IG from 1/2 to 1/10 to lie below the level in the control wafers. (2) Breakdown voltage recovery, with histograms of breakdown voltage for threshold current I_{th} = 1 μA (where the electric field is about 12 MV/cm) depicted in Fig. 6. Breakdown voltage evidently recovers by several volts.

Reduction in the leakage current of the oxide films in the low electric field by IG has yet to be reported, and furthermore, the mechanism is not clear. Such reduction may be achieved by a mechanism similar to that concerning recovery in breakdown voltage discussed below.

The IG effect on oxide film breakdown is considered to be as follows: A possible origin of the breakdown degradation is contamination (Fig.7(a))

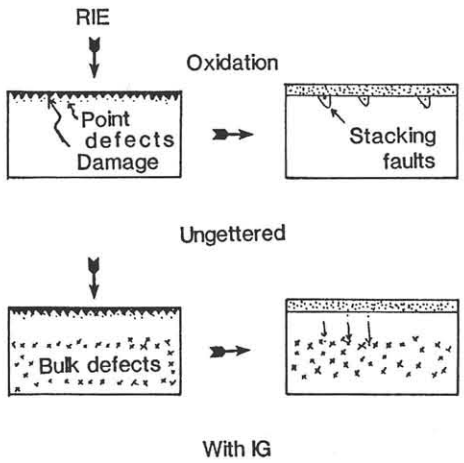

Fig. 4. A model for defect generation by RIE damage and gettering the damage by IG.

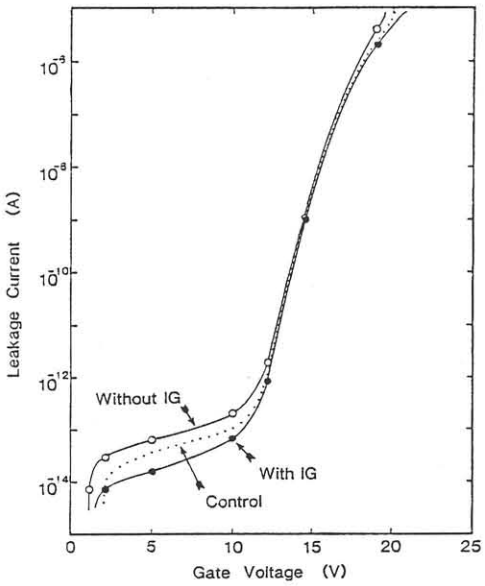

Fig. 5. Typical current-voltage characteristics for oxide films of IG, ungettered and control wafers.

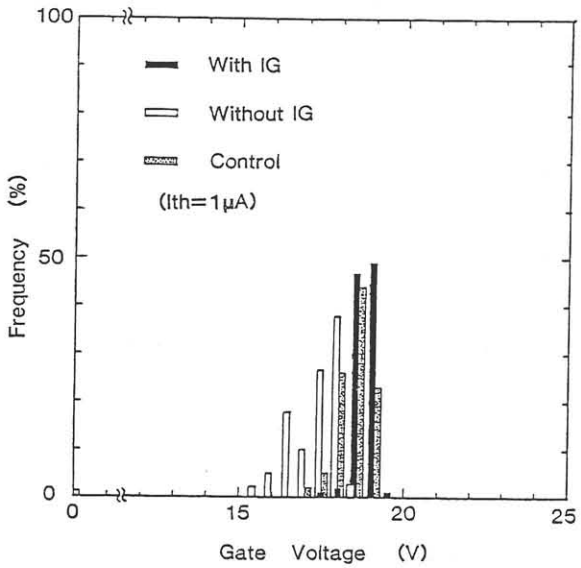

Fig. 6. Histograms of breakdown voltage of 15 nm thick oxide films. Threshold current is set at 1 μA.

or structural defects (Fig. 7(b)) in the oxide films. The latter model is unsuitable by the following reasons. Structural defects in the substrates such as oxide precipitates, incorporated into the oxide films during oxidation, are reduced by high-temperature annealing. This defect reduction will in turn result in improvement on breakdown voltage of the oxide films. However, this cannot explain the present results. Precipitates exist approximately 10^6 cm^{-3} in density in CZ crystals.[10] Only defects less than 1 cm^{-2} would be included in the oxide, which is one order of magnitude lower than typical oxide defect density. Further, it has been confirmed that oxide precipitates intentionally introduced at the oxide-substrate interface do not increase the oxide leakage.[9] On the other hand, defect density was higher in oxide film on CZ wafers than in that on FZ wafers, which might be due to metallic impurities in the former wafers.[7] High-temperature, long-term annealing might also increase the contamination. Consequently, contamination due to impurities in the substrates or high-temperature annealing should constitute the origin of the oxide breakdown. Thus, the remarkable IG effect was observed.

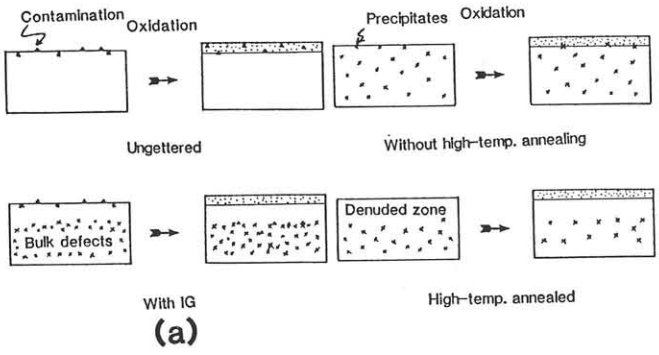

Fig. 7. Models for breakdown voltage degradation and its prevention in oxide films.
(a) A contamination-gettering model.
(b) A precipitation-denuded zone model.

4. Conclusion

The IG effects on two problems in forthcoming VLSI processing were examined and confirmed as follows: (1) The minority carrier lifetime of reactive ion etched IG substrates was maintained at more than a few hundred microseconds even with an ion acceleration voltage as high as 1000 V, while that of ungettered substrates decreased below a few microseconds. (2) Current leakage in the 15 nm-thick oxide films formed after high-temperature long-term annealing was suppressed to the level comparable to that in the 50 nm-thick oxide films formed on the substrates without high-temperature pre-annealing. Possible mechanisms for these two kinds of degradations and the IG effects on them were discussed as well.

Acknowledgments

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