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Improved CMOS Device Performance through Silicon Epitaxial Intrinsic Gettering Techniques

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Improved silicon epitaxial layers have been achieved by applying intrinsic gettering techniques to the epi/substrate wafer. These gettering techniques have been investigated for both N-well and P-well CMOS technologies using P on P+ and N on N+ epitaxial structures. Epitaxial gettering was observed to be dependent on the substrate wafer defect properties. Through the proper gettering technique, use of silicon epitaxial structures for CMOS device processing improves device latch-up immunity, gate oxide integrity, and diode junction quality thereby enhacing device yields.

1. Introduction

As CMOS devices are scaled to the micron and sub-micron levels for increased device packing density, they become more susceptible to latch-up. A solution to latch-up at these minimal device geometries is the use of epitaxial wafers. Troutman et al. (1) reported improved latch-up immunity in an N-well CMOS process by using P on P+ epi-wafers. Yamaguchi et al. (2) also reported latch-up free CMOS devices at 0.5 micron level by using N on N+ epi-wafers. Although the use of epi-wafers will improve CMOS latch-up immunity, the quality of the epilayer will also directly affect other device parameters and yield. Crystallographic defects ranging from impurity atoms to macro-dislocations located in the device active region can degrade the device. Therefore, high quality silicon epitaxial wafers free of impurities and defects must be realized in order for these advanced CMOS devices to be a reality in today's high volume production world.

Gettering in silicon to remove impurities from the near surface device active region and trapping them in the bulk of the wafer has been described in numerous publications (3, 4, 5, 6, 7). Intrinsic gettering is a technique of using the super-saturated interstitial oxygen (Oi) present in Cz-grown silicon wafers and inducing SiOx precipitation by thermal annealing. These precipitates generate lattice disorder and defects which act as traps (getter sites) for impurities. The application of intrinsic gettering techniques to lightly doped N and P bulk wafers is well documented. For CMOS/Epi technology, heavily doped N+ and P+ wafers are used as epitaxial substrates where the interaction of the substrate intrinsic material properties with the oxygen precipitation gettering mechanism is not totally understood (8, 9, 10, 11). Therefore, the focus of this paper is to present some recent results on improved CMOS silicon epitaxial layer quality through the application of intrinsic gettering techniques to P+ and N+ (100) wafers.

2. Epitaxial Intrinsic Gettering Techniques

Silicon epitaxial intrinsic gettering for CMOS device processing can be divided into either pre-epitaxial gettering or post-epitaxial gettering techniques. The intrinsic gettering mechanism can be activated in the substrate wafer prior to or after silicon CVD epitaxial growth. In this investigation, pre-epitaxial gettering was achieved by subjecting the substrate wafers to a high-low-medium 3-step intrinsic gettering cycle (12). Post-epitaxial gettering was achieved by subjecting the epi-wafers to an SiOx precipitate nucleation and growth cycle prior to device processing.

For the P-well CMOS process, heavily doped antimony, 0.01 Ω-cm, (100) orientation, 76mm wafers were used for N+ substrates. Phosphine doped epilayers, 4 Ω-cm, 8 μm thick were grown at 1150°C using $SiCl_4$. The N-well CMOS process used heavily doped boron, 0.01 Ω-cm, (100) orientation, 100mm wafers for P+ substrates. Boron doped epilayers, 6 Ω-cm, 10 μm thick were grown at 1130°C using $SiCl_4$.

Wafer split lots were compared using a 3 μm P-well CMOS process and a 1.25 μm N-well CMOS process. Both non-gettered and intrinsically gettered epi-wafers were investigated. The results of the split lot comparison are presented in the following section.

3. Results

3 μm P-well CMOS Technology:

Wright etchant (13) defect analysis consistently revealed high density of epi-surface shallow etch pits (>10^5 pits/cm^2) on non-gettered N on N+ epi-wafers (See Figure 1). In addition, MOS capacitance-time epilayer minority carrier

lifetime measurements were usually less than 10 μsec. By subjecting N+ wafers to the pre-epitaxial gettering technique, the epi-surface shallow etch pits were eliminated and epilayer lifetimes improved by over an order of magnitude. (See Figure 2).

CMOS devices were fabricated to determine the interaction of these epilayer micro-defects on device performance. Latch-up results for the P-well CMOS technology comparing bulk wafers to epi-wafers is shown in Figure 3. N-bulk intrinsic gettering improves latch-up immunity as was reported by Sakai et al. (14). The bulk SiOx precipitates reduced B_V by lowering the bulk lifetime and B_L increased due to the high crystalline perfection near the wafer surface. The net result was a doubling in the holding current. Use of N on N+ epi-wafers reduced B_V and had no significant effect on B_L, however, all of the devices fabricated on epi-wafers were latch-up free. Therefore, the epilayer micro-defects seem to have no detectable impact on latch-up performance.

Besides latch-up data, junction breakdown voltage was also measured at a fixed 20 micro-Amps of current on $1mm^2$ diodes. These results are shown in Figure 4. Non-gettered N on N+ epi-wafers had poor diode characteristics while both pre-epitaxial and post-epitaxial gettered wafers had diode characteristics better than N-bulk wafers and equal to intrinsic gettered bulk wafers. This measurement technique seems to be more sensitive to the epilayer micro-defects.

Die per wafer yield on the P-well CMOS circuit performance was tabulated and normalized in Figure 5 to the N-bulk wafers as the control. The criteria for circuit performance yield was a leakage current (I_{DD}) of less than 250 micro-Amps. The Non-gettered epi-wafers had zero yield due to the interaction of the epilayer micro-defects on circuit performance. The pre-epitaxial gettering treatment improved circuit yield to 0.75 while intrinsic gettered N-bulk wafers improved yield to 1.75. Although N on N+ epi-wafers are needed to eliminate latch-up in this P-well CMOS process, the epilayer micro-defects resulted in the degradation of device circuit yield. Application of epitaxial gettering techniques to N on N+ epi-wafers are required to yield good CMOS device circuit performance.

1.25 μm N-well CMOS Technology:

Unlike N on N+ epi-wafers, non-gettered P on P+ epi-wafers were free of epi-surface shallow etch pits. Defect analysis results showed that neither pre-epitaxial gettering nor post-epitaxial gettering treatments are required since high concentrations of boron dopant in the P+ substrate wafers provide effective process induced gettering during the subsequent device fabrication process flow (12). The denuded zone with bulk intrinsic gettering sites induced during the N-well CMOS process is shown in Figure 6. The epilayer lifetime was in the millisecond range. Therefore, for this particular N-well process flow, process induced gettering is sufficient and no additional epitaxial gettering is required.

Latch-up analysis comparing CMOS/bulk to CMOS/Epi technology is shown in Figure 7. For this N-well CMOS technology, use of P on P+ epi-wafers doubled B_L and improved I_H by 1.6 times. Pre-epitaxial gettering increased B_L and I_H even more than the non-gettered epi-wafer values. The electric field induced by the high-low junction formed at the epi/substrate dopant transition region increased the lateral current flow and the combination of this effect with the reduced substrate resistance resulted in the improved latch-up immunity in epi-wafers. (1, 12) The combination of increased lateral beta in epitaxial gettered wafers due to improved epilayer lifetime and bulk gettering sites resulted in the improved I_H.

Gate oxide integrity was used to characterize the silicon wafer quality. Particles and contaminants as well as defects (metallic impurities and micro-defects) located at or near the wafer surface are incorporated into the growing oxide resulting in oxide defects and pin holes. The degradation of the thin gate oxide (200Å) results in intermediate breakdown voltages which are lower than the intrinsic breakdown voltage. Preliminary results revealed intermediate breakdown voltages on all P-type bulk wafers down to 11 volts as shown in Figure 8. All of the P on P+ epi-wafers showed excellent gate oxide breakdowns. Process induced gettering resulted in the high crystalline quality of the silicon epilayer which gave rise to the excellent breakdown histograms. Therefore, no special epitaxial gettering technique is required to achieve excellent gate oxide quality on P on P+ epi-wafers.

4. Summary

Use of N on N+ and P on P+ epitaxial wafers for advanced CMOS processing can provide very effective latch-up immunity. However, epitaxial micro-defects can degrade other CMOS device parameters. This is especially evident in N on N+ epi-wafers. Crystallographic imperfections in the epilayer have been eliminated through epitaxial intrinsic gettering techniques. This has resulted in improved lifetime, diode junction quality and yield enhancement in the 3 μm P-well CMOS process. No special epitaxial gettering was required in the 1.25 μm N-well CMOS process due to very effective process induced gettering. Excellent gate oxide integrity was observed on P on P+ epi-wafers. In conclusion, incorporating epitaxial intrinsic gettering techniques into CMOS/Epi processing will improve latch-up immunity, diode junction quality and gate oxide integrity thereby enhancing device yield.

5. References

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FIG. 1: N on N+ Epilayer Surface After Wright Etch

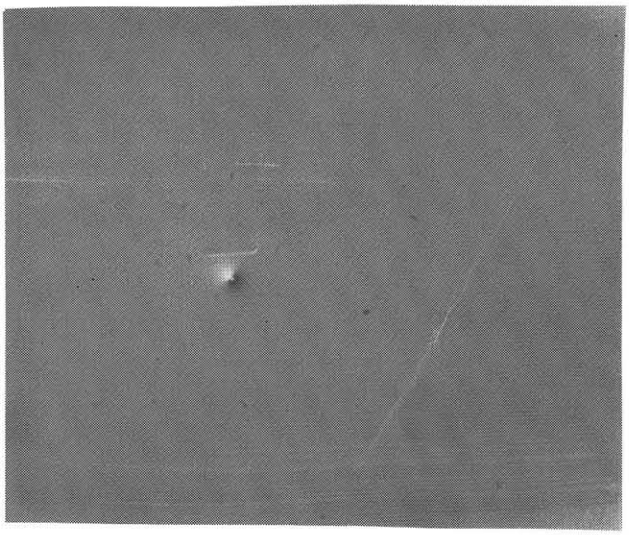

FIG. 2: Gettered N on N+ Epilayer Surface after Wright Etch

	B_V	B_L	I_H (mA)
N-Bulk	60	.18	20
N-Bulk IG	52	.22	40
Epi	48	.21	No Latch-up
Pre-Epi IG	50	.16	No Latch-up
Post-Epi IG	50	.21	No Latch-up

FIG. 3: P-well Latch-up (3 μm Design Rule)

	N+ to P-well	P+ to Substrate
N-Bulk	15.5 ± 3.5	45.4 ± 10.4
N-Bulk IG	16.6 ± 2.9	41.8 ± 10.0
Epi	12.7 ± 3.9	41.9 ± 13.6
Pre-Epi IG	16.3 ± 3.3	43.6 ± 9.3
Post-Epi IG	16.8 ± 4.8	44.4 ± 13.4

FIG. 4: Diode Junction Breakdown Voltage

	Normalized Yield
N-Bulk	1.0
N-Bulk IG	1.75
Epi	0.0
Epi Pre-IG	0.75

FIG. 5: Normalized Yield on Circuit Performance

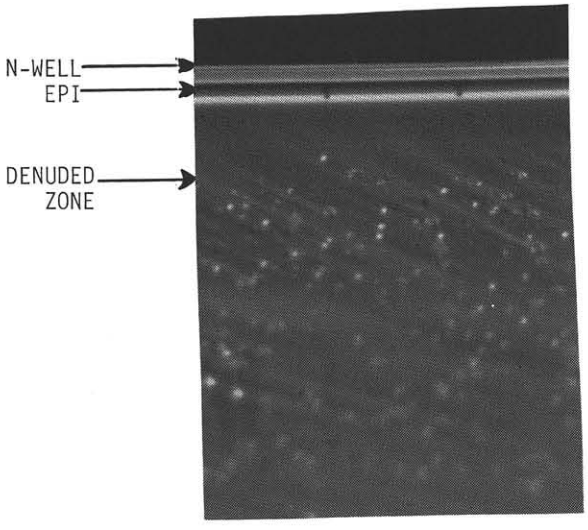

FIG. 6: Process Induced Gettering in an N-well CMOS Process Flow.

	B_V	B_L	I_H (mA)
P-Bulk	24.8	2.2	4.4
Epi	27.6	5.0	7.3
Pre-Epi IG	25.4	5.2	12.4

FIG. 7: N-well Latch-up (1.25 μm Design Rule)

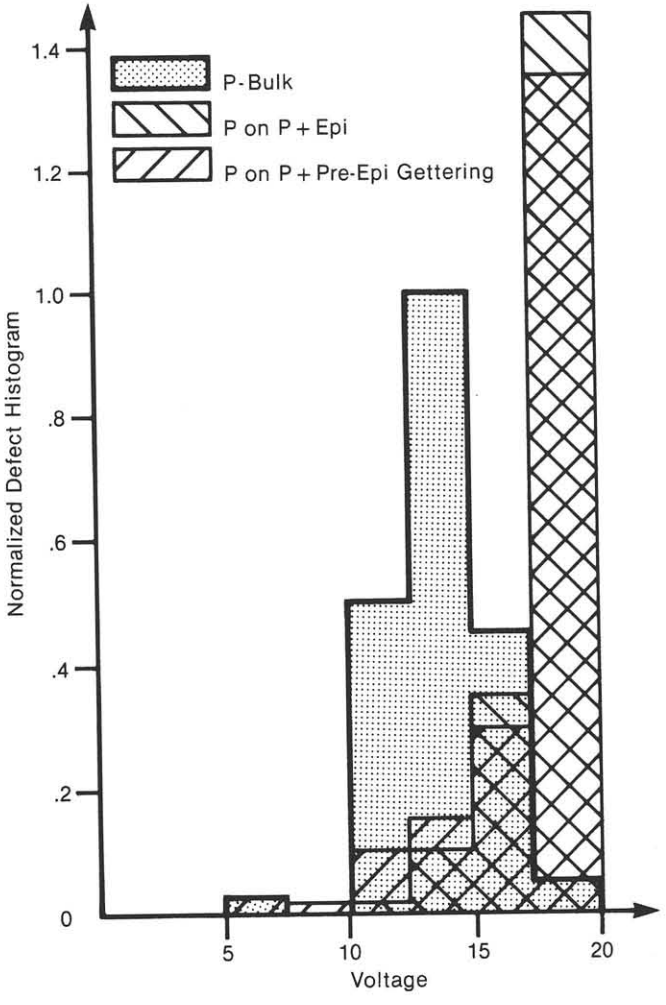

FIG. 8: Gate Oxide Integrity