Extended Abstracts of the 16th (1984 International) Conference on Solid State Devices and Materials, Kobe, 1984, pp. 15-18

Invited

Refractory Metals and Silicides for Si MOS VLSI's

S. Iwata
Central Research Lab., Hitachi, Ltd.
Kokubunji, Tokyo

Various properties of refractory metals and their silicides are first compared. Then, some of the problems encountered when using metals like Mo and W are discussed. The stability of metal/SiO_2/Si at high temperatures is compared for these metals, showing W to be superior to Mo as a gate metal. It is also shown that mobile ion contamination can be made extremely low in vacuum-melted sputter targets of these metals, making these refractory metals very attractive for VLSI use.

I. Introduction

With the increase in the integration density of LSI's, refractory metal silicides are beginning to be used in place of poly Si for MOS gates and interconnects. This is due to the increase in the RC delay, if poly Si, which has low electrical conductivity, is to be used. Furthermore, in the near future when VLSI's of megabit level appears, it is expected that pure refractory metals, with higher conductivity, will be used, replacing poly Si and metal silicides.

In this paper, various properties of these metals and their silicides will first be compared as materials for VLSI applications. Then, some of the problems encountered when using such metals as Mo and W will be discussed.

II. Materials for future VLSI's

Many requirements must be satisfied if a material is to be used as MOS gates and interconnects. Among the properties to be considered are electrical conductivity, heat resistance, adhesion to SiO_2, oxidation resistance, gate material/SiO_2/Si stability, and low impurity content. A comparison of some of these properties for refractory metals, their silicides, and poly Si is shown in Table 1.

At present, silicides/poly Si("polycide")/SiO_2 Si MOS structures using such silicides as $MoSi_2$, WSi_2, etc. are being considered or used for MOS VLSI's.[1)-3)] The sheet resistance for these polycides is 1-10 Ω/□. However, it is considered imperative that silicides without poly Si underneath or refractory metals will be used for megabit-level VLSI's.[4)] Some of the problems associated with using these metals will next be discussed, since their eventual use is inevitable, there are many problems for these metals, and many studies have already been reported on silicides.[1)-3)]

III. Problems for refractory metals

The sheet resistance well below 1 Ω/□ is possible if such metals as Mo and W are used.[5)-7)] However, there are many problems to be solved before they can be used. Although these metals have high conductivity and high melting point,

Table 1 Comparison of materials for VLSI

material	silicon	polycide	silicide	pure metal	
examples	poly Si	$MoSi_2$/poly Si $TaSi_2$/poly Si WSi_2/poly Si, etc.	$MoSi_2$, $TaSi_2$, WSi_2, etc.	Mo	W
electrical resistance (Ω/□)	poor (~30)	fair (1~10)	fair (1~10)	good (<1)	good (<1)
adhesion to SiO_2	good	good	good	fair ~good	good (sputtered W)
material/SiO_2/Si stability	good	good	fair ~good	fair ~good	good
oxidation resistance	good	fair ~good	fair	poor	poor

i) they cannot withstand high-temperature oxidizing ambients, ii) they cannot be used as mask against ion channeling during ion implantation for a self-aligned gate process, and iii) many studies regarding reliability are still required.

A number of studies have been reported on the sclution of the first two problems.[6),7)] In all these studies, sputtered Mo or W is used, because of the fairly good adhesion to SiO_2 obtained by sputtering. Oxidation of these metals can be prevented if annealing is carried out in an inert or reducing ambient. However, Si cannot be oxidized in this ambient, as is done in the conventional Si process. A new heat treatment using a H_2/H_2O ambient makes this Si oxidation possible without oxidizing these metals.[7)] Ion channeling during ion implantation can be prevented by forming a layer of PSG or WO_x on W,[7)] or by nitriding Mo.[6)]

The problems connected with reliability, namely, the stability of the metal/SiO_2/Si structure will now be considered.

(1) High-temperature stability of metal/SiO_2/Si

As gate oxides become thinner, the stability of metal/SiO_2/Si becomes extremely important, since any reaction involving the metal, SiO_2, and Si may result in the degradation of MOS characteristics. Accordingly, the stabilities of Mo/ and W/SiO_2/Si were compared as follows:

First, these two structures were annealed at 500-1100°C, and their surfaces were examined by ESCA. The analysis indicated the presence of Si on the surface of Mo/SiO_2/Si after annealing in N_2 at 1100°C (1000°C in H_2), whereas no Si was detected on the surface of W/SiO_2/Si.

Secondly, surface analysis of SiO_2, after chemically removing the metals, showed the SiO_2 thickness to be decreased for Mo/SiO_2/Si after annealing at 1000°C in H_2, whereas no such changes were observed for W/SiO_2/Si, as shown in Figs. 1 and 2. This thickness was obtained from the intensity ratio of oxidized and unoxidized Si peaks (by ESCA). This thickness decrease is believed to be due to localized reduction of SiO_2, rather than a uniform decrease in the SiO_2 thickness.

Corresponding to these results, the breakdown

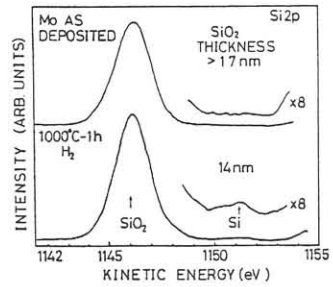


Fig.1 Si2p spectra for SiO_2 surface in Mo/SiO_2/Si

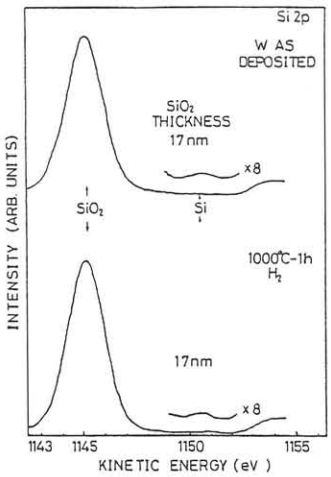


Fig.2 Si2p spectra for SiO_2 surface in W/SiO_2/Si

voltage of the W/SiO_2(20 nm thick)/Si structure was found to be about 6 V, as compared with 1 V for the Mo/SiO_2/Si structure, after annealing at 1000°C for 1 h in H_2. These results and the fact that adhesion to SiO_2 was better for W than for Mo[7)] show W to be more suitable for a gate metal than Mo.

(2) Mechanism of metal/SiO_2/Si reaction

It was first thought that the above results were due to metal/SiO_2 reactivity. However, this conclusion became doubtful when the following points became clear:

i) Si, found on the surface of Mo/SiO_2/Si, was all oxidized Si, even if annealing was done in vacuum ($1x10^{-5}$Pa), where Si is usually not much oxidized.

ii) SiO_2 could be reduced to Si in H_2 if H_2O content was less than a few ppm. This reduction became less if there was Mo on the SiO_2, and less so if the metal on the SiO_2 was W.

iii) When any instability of the Mo/SiO_2/Si structure was observed, more changes were found inside the SiO_2 nearer to the SiO_2/Si interface than at the Mo/SiO_2 interface Fig. 3 shows the

difference in the Si2p ESCA spectra at a distance of 5 nm from the SiO_2/Si interface after annealing in H_2 and in N_2. For Mo/SiO_2/Si annealed in H_2, the SiO_2 was found to be partially reduced to SiO_x (x<2), indicating Mo/SiO_2/Si to be less stable in H_2 than in N_2. This is supported by the result shown in Fig. 4, which indicates that, after annealing in H_2, the O-to-Si ratio in the oxide becomes less than that for SiO_2 as the SiO_2/Si interface is approached.

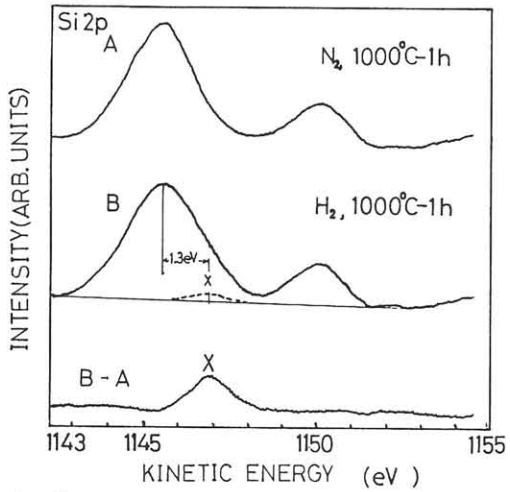


Fig.3 Comparison of Si2p spectra for SiO_2(5 nm from SiO_2/Si interface;see Fig.4) after annealing in N_2 and H_2

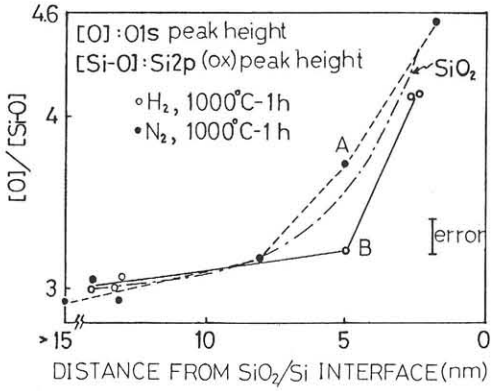


Fig.4 Depth profile of O1s/Si2p(oxidized) ESCA peak ratio inside SiO_2 in Mo/SiO_2/Si

iv) MoO_x or WO_x is found at the metal/ SiO_2 interface after deposition.[7] This MoO_x can be partly reduced to Mo if annealed in H_2 at 1000°C for 1 h, but the WO_x cannot be reduced by this annealing. This oxide possibly has an influence on the stability of the metal/SiO_2/Si structure.

v) Thermodynamic data show that both Mo and W are not reactive with SiO_2,[8] as also expected from the study of Pretorius et al.[9] They also show that a reaction between SiO_2 and Si to form SiO, or that between SiO_2 and H_2 may occur at around 1000°C.[8]

These data suggest that a reaction between SiO_2 and Si to form SiO (or SiO_x) or that between SiO_2 and H_2 may be more important than a metal/SiO_2 reaction. Furthermore, metal oxides, present at metal/SiO_2 interfaces, are considered to provide an oxidizing "atmosphere" for the various reactions which may occur in the metal/SiO_2/Si structure, making SiO_2 more stable by their presence.

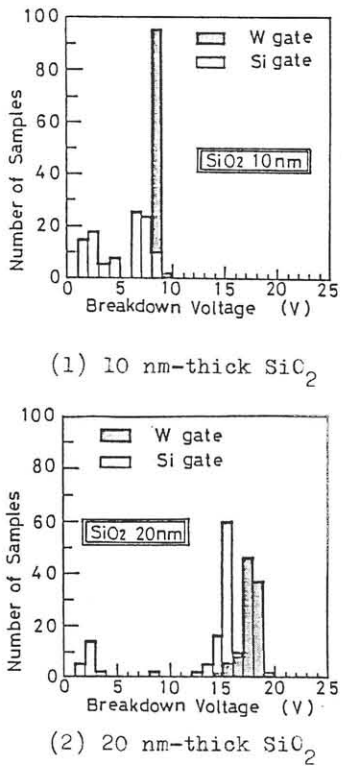


Fig.5 Comparison of breakdown voltages for W- and Si-gate MOS

Finally, the breakdown voltages are compared for W* and Si gate MOS diodes with 10 or 20 nm-thick SiO_2 in Fig. 5. The figure shows the superiority of W as a gate material for use in VLSI's with thin SiO_2.

* annealing done in N_2 with a few ppm of O_2

(3) Mobile ion contamination in metal/SiO_2/Si

Mobile ion contamination must be kept low if a metal is to be used as a gate material. It is reported by Amazawa et al.[10] that Na and U contents as low as 30 and 5 ppb, respectively, are realized in a vacuum-melted sputter target supplied by Nippon Mining Co.

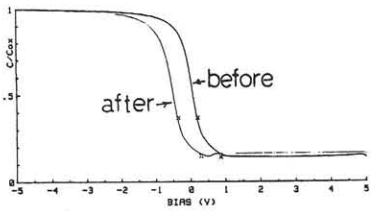
Low Na and U contents can also be achieved for W (also by the same company). The results of chemical analysis for this W target is shown in Table 2, together with those for a commercially available conventional target. The table also

Table 2 Comparison of conventional and high-purity W targets

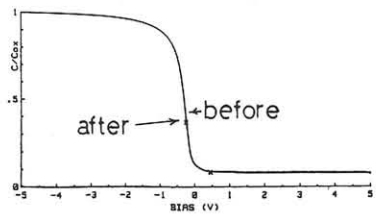
target	impurities(ppm)			ΔV_{fb} (V)+
	Na	K	U	3 MV/cm-200°C-30min
conventional	10-100		0.1	0.5 ~ 2
high-purity	0.01 ~0.02	<0.05	0.005 ~0.007	0

+ no PSG on W; error ± 0.02 V

shows the change in the flat-band voltage ΔV_{fb} after a BT (bias-temperature) test for MOS diodes with W sputtered from these targets. Fig. 6 shows the C-V (capacitance-voltage) curves before and after a BT (3 MV/cm-200°C-30 min) stress for the conventional and high-purity targets. ΔV_{fb} for the MOS diodes fabricated using the latter was 0 V, compared with 0.5 V for the former.



(1) Conventional target



(2) High-purity target

Fig.6 Comparison of C-V curves for W-gate MOS before and after a BT stress (3 MV/cm-200°C-30 min)

III. Conclusions

Various properties of refractory metals and their silicides for VLSI applications were discussed with emphasis on the stability of gate material/SiO_2/Si in regard to high-temperature annealing and mobile ion contamination. It was shown that W/SiO_2/Si was more stable than Mo/SiO_2/Si during this annealing. Regarding mobile ion contamination, such impurities as Na in Mo or W can be made as low as 30 ppb or less, so that no shifts in V_{fb} are observed after a BT test.

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